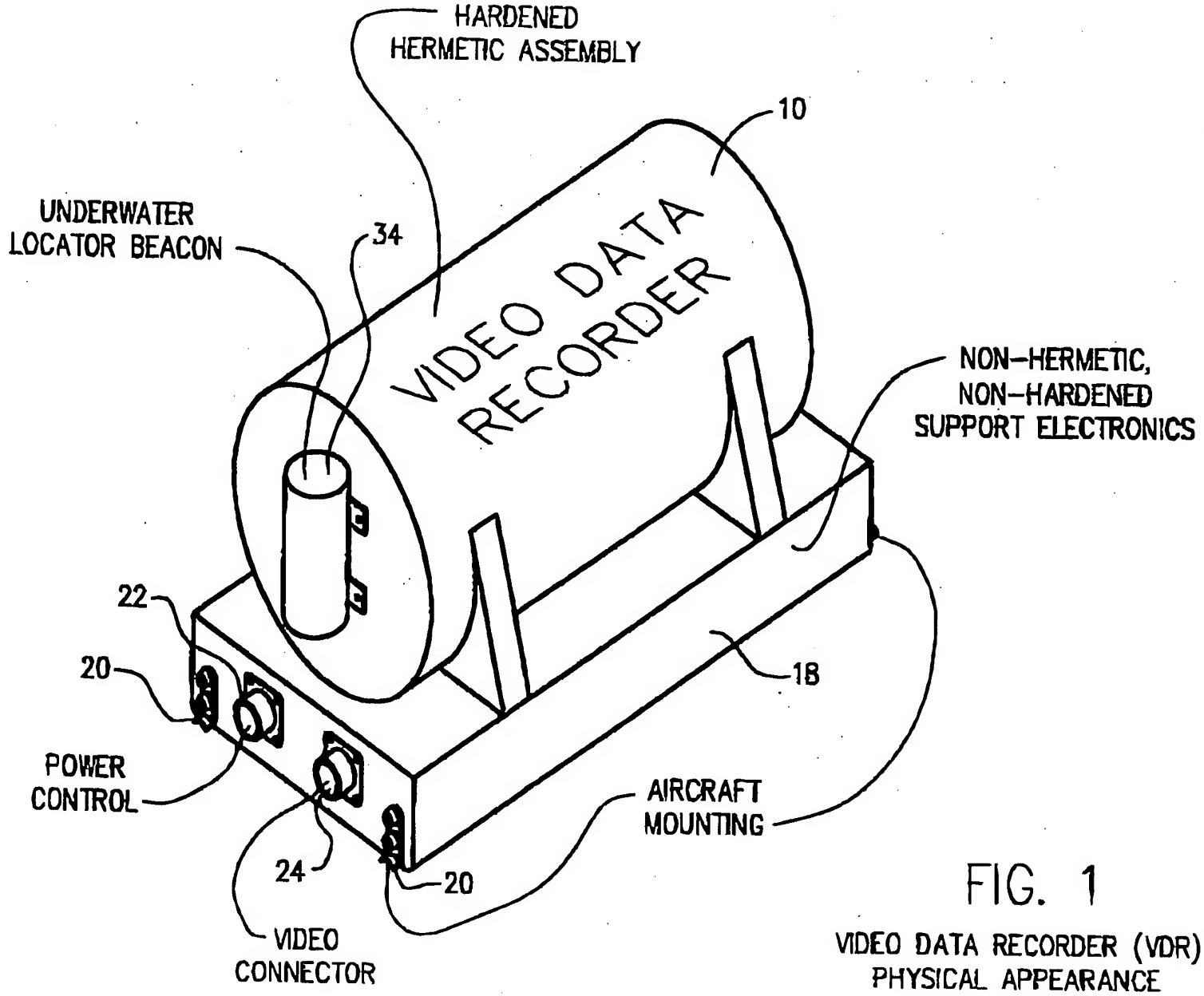


FIG. 1

VIDEO DATA RECORDER (VDR)
PHYSICAL APPEARANCE

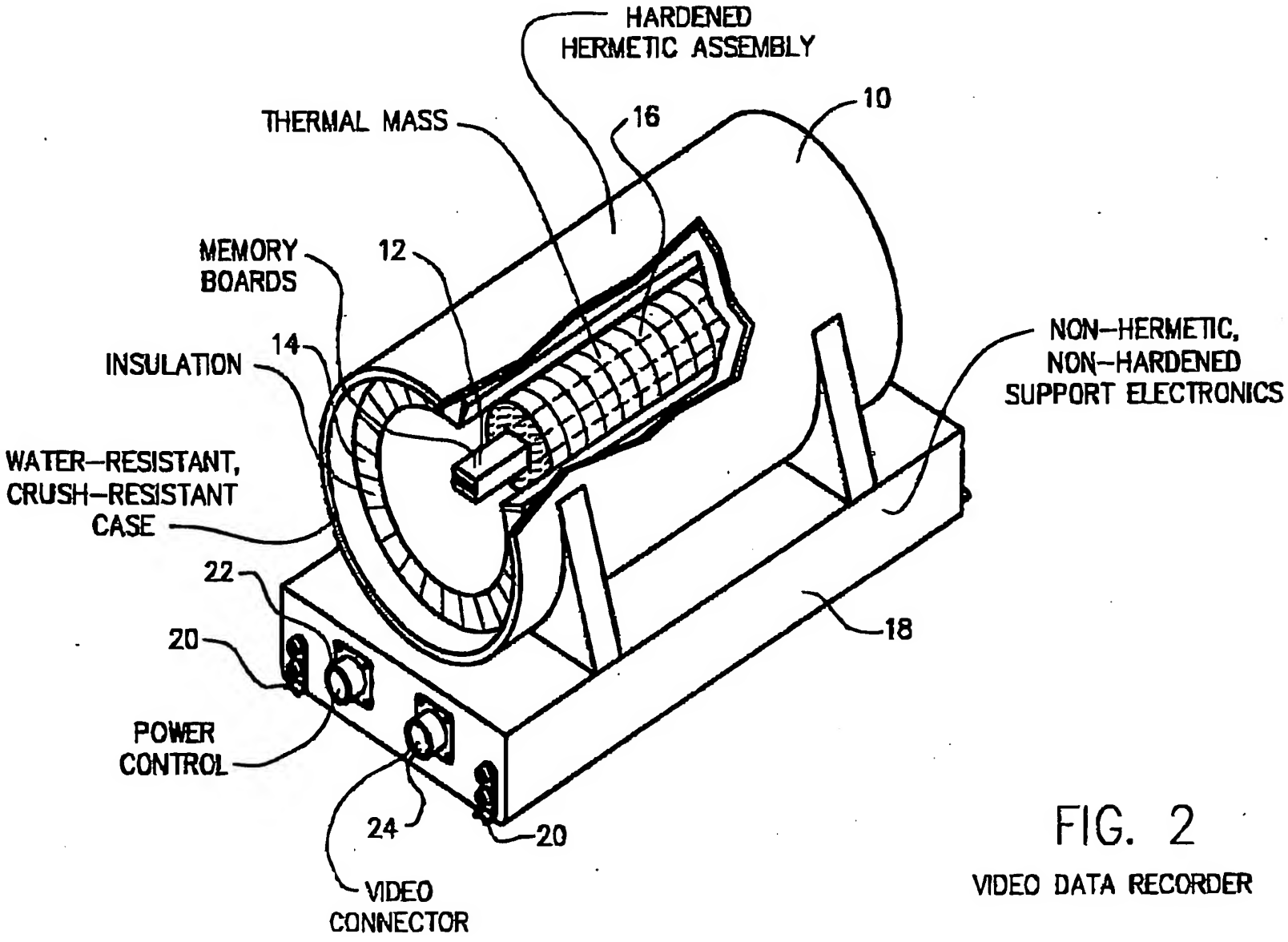


FIG. 2

VIDEO DATA RECORDER

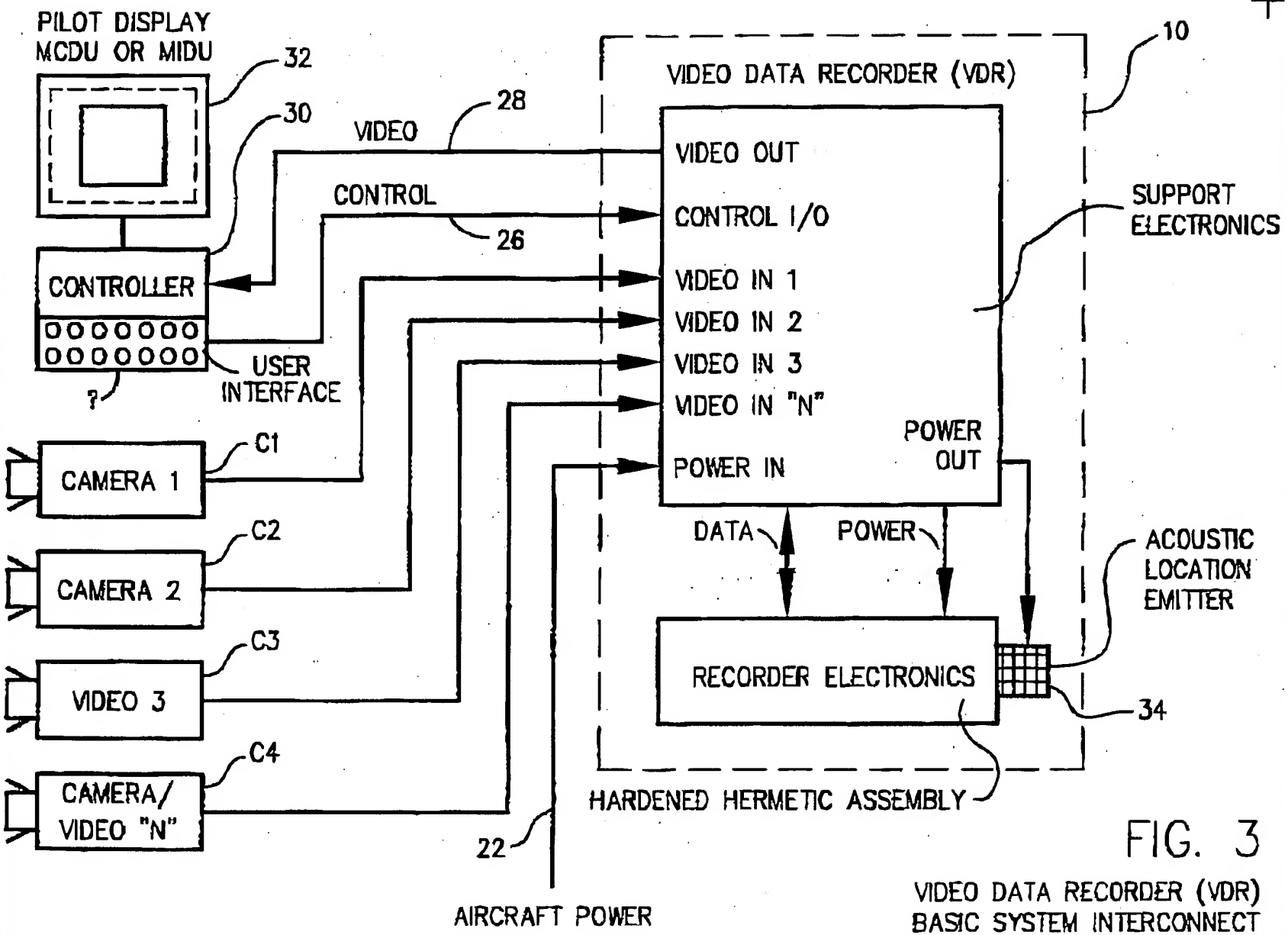


FIG. 3

VIDEO DATA RECORDER (VDR)
BASIC SYSTEM INTERCONNECT

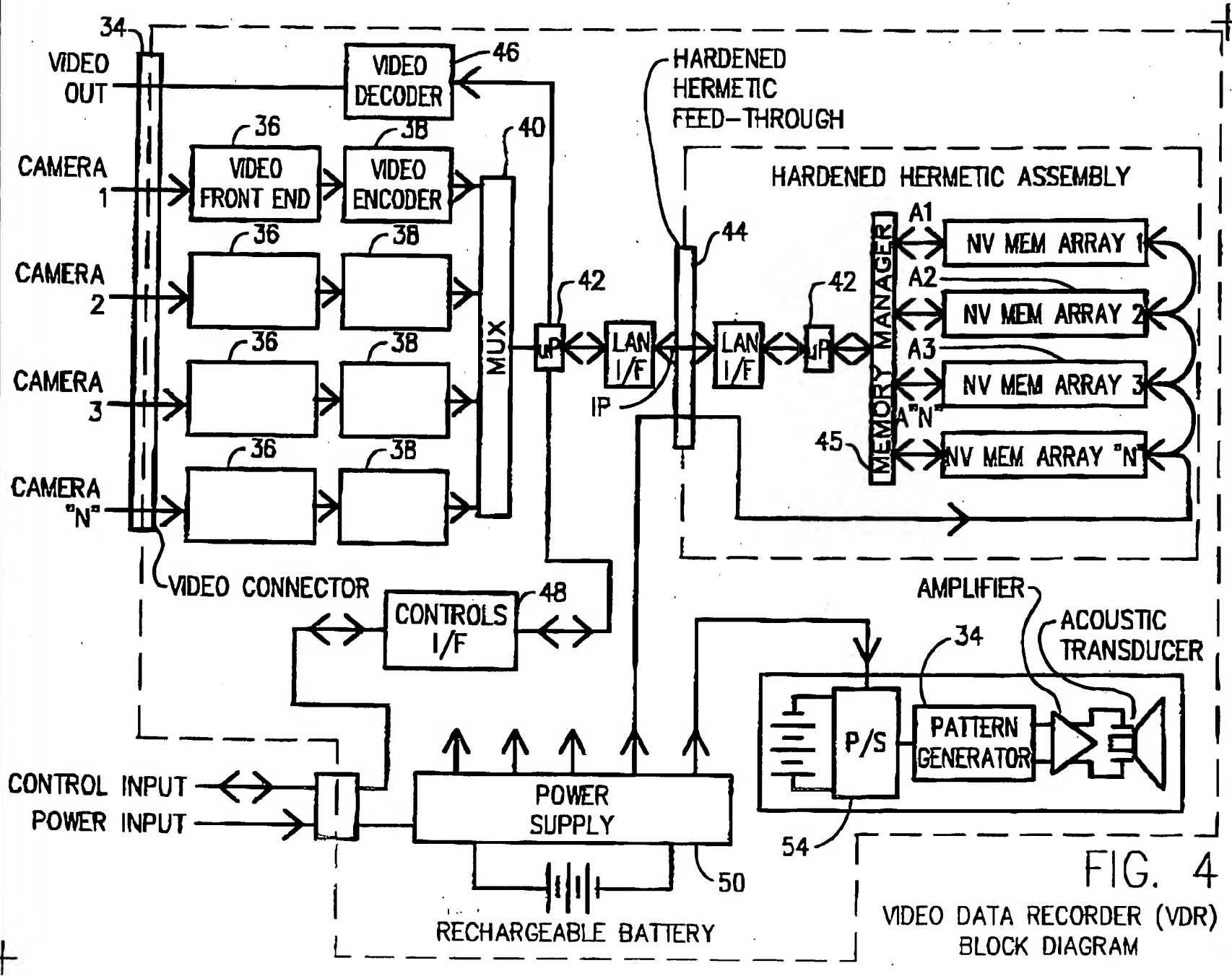


FIG. 4

VIDEO DATA RECORDER (VDR) BLOCK DIAGRAM

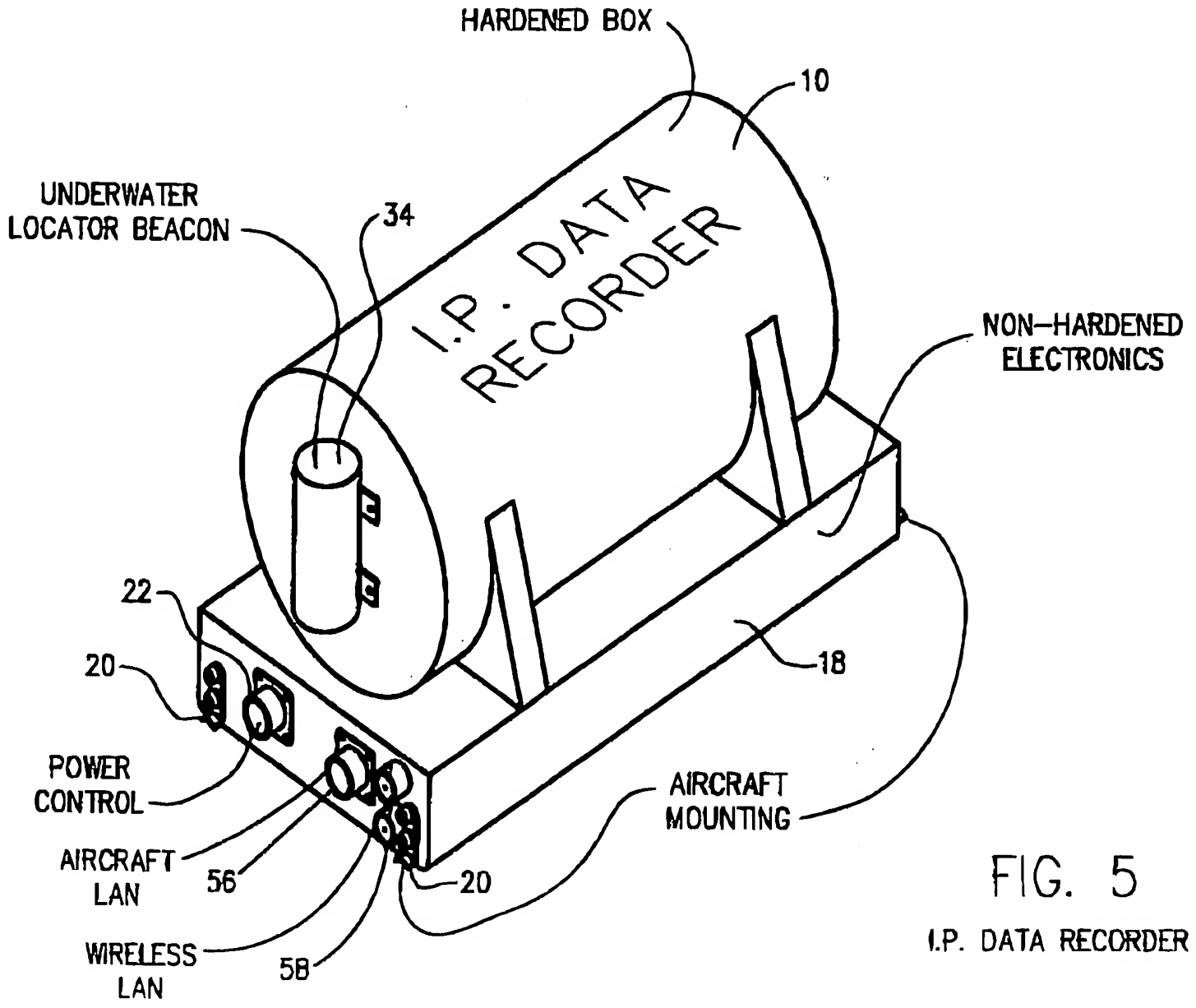


FIG. 5

I.P. DATA RECORDER

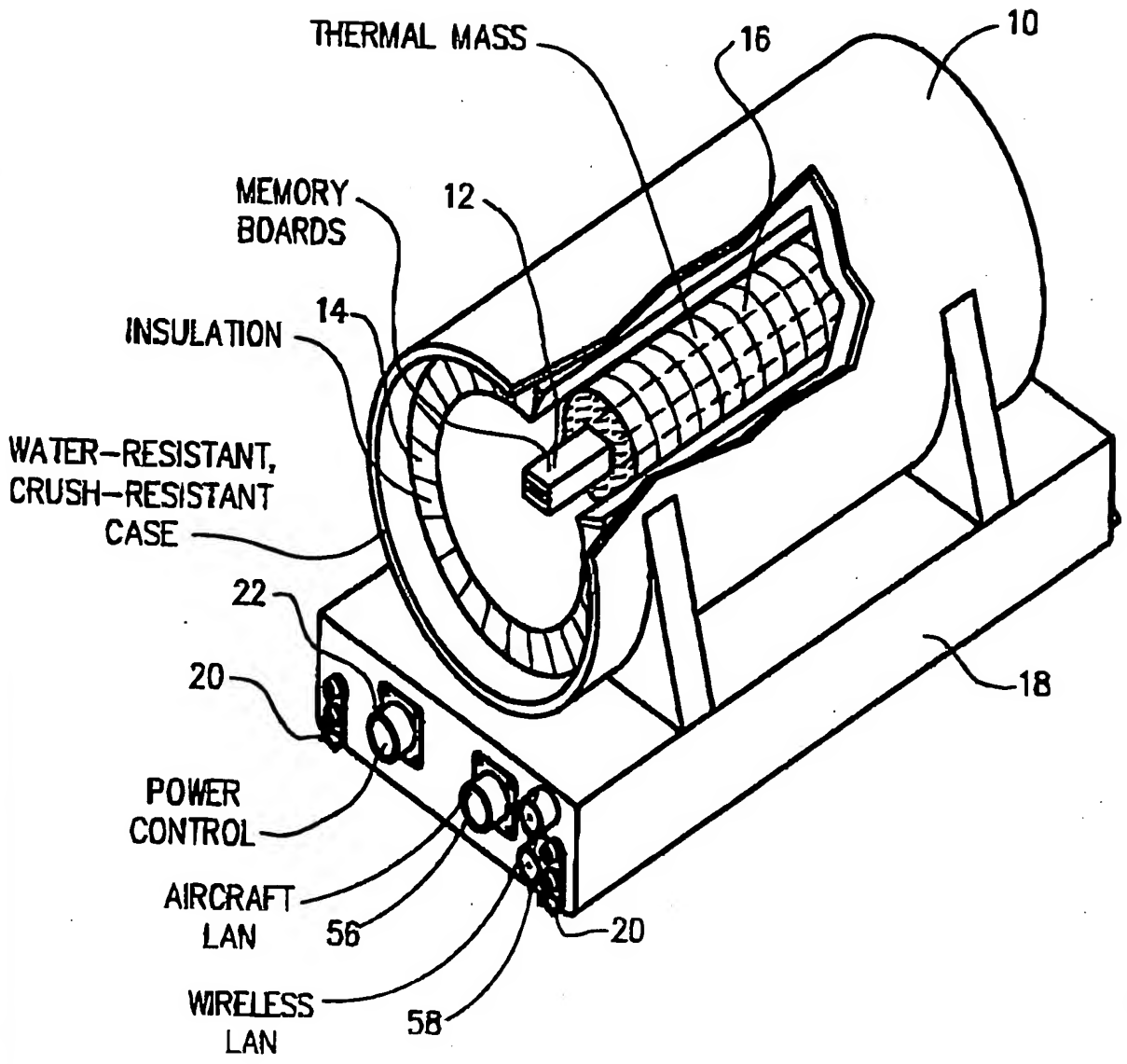


FIG. 6

I.P. DATA RECORDER

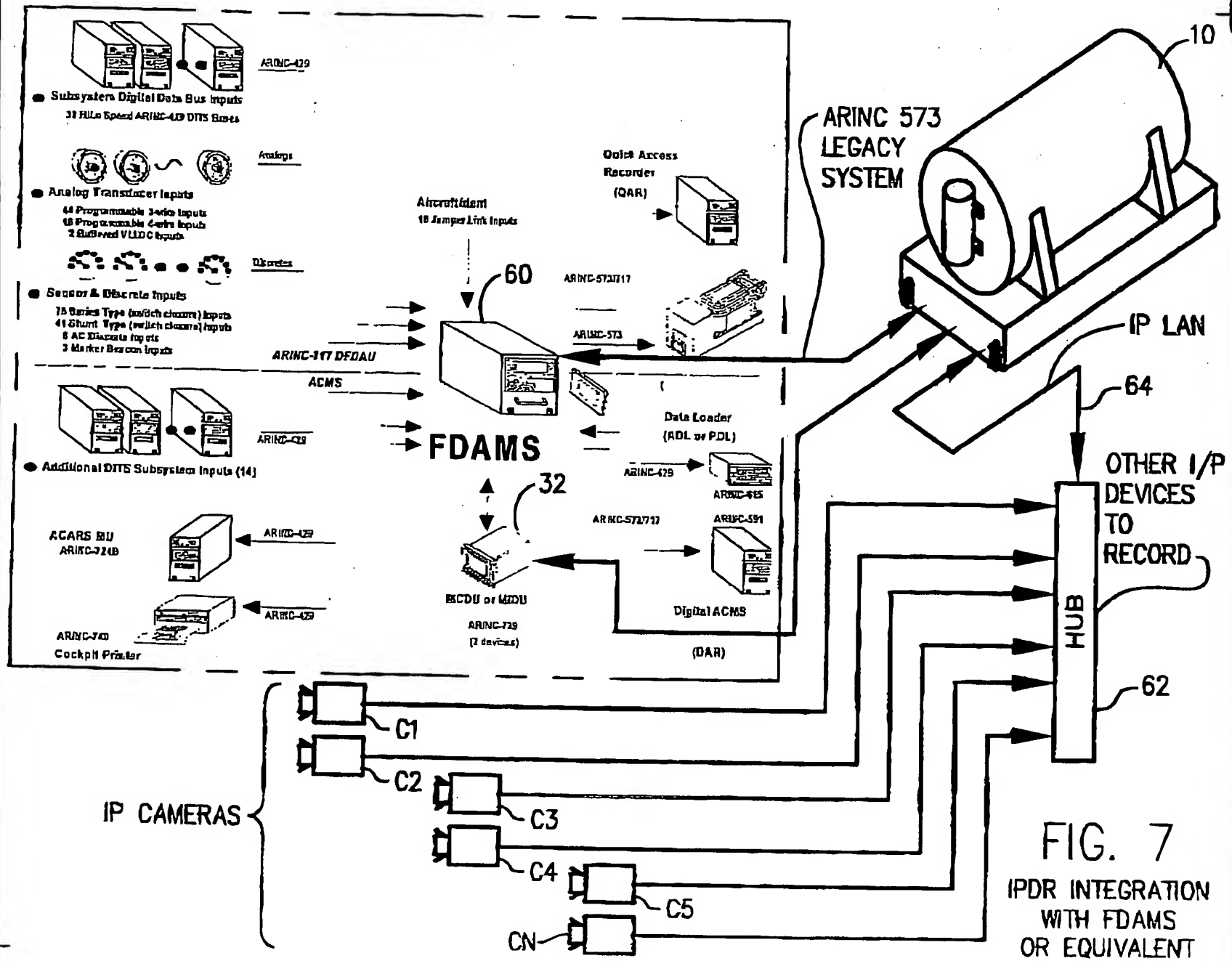


FIG. 7

IPDR INTEGRATION WITH FDAMS OR EQUIVALENT

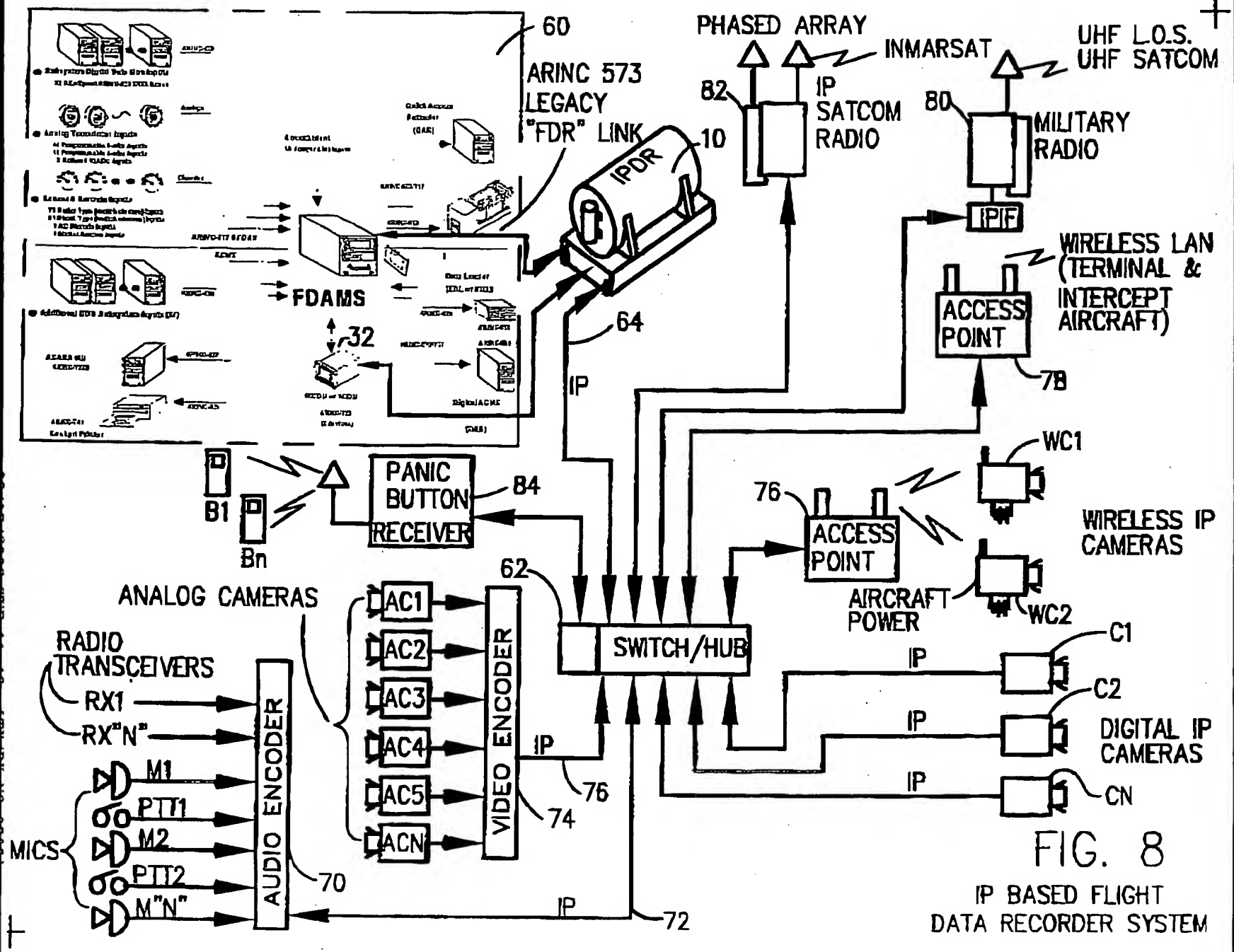


FIG. 8

IP BASED FLIGHT
DATA RECORDER SYSTEM

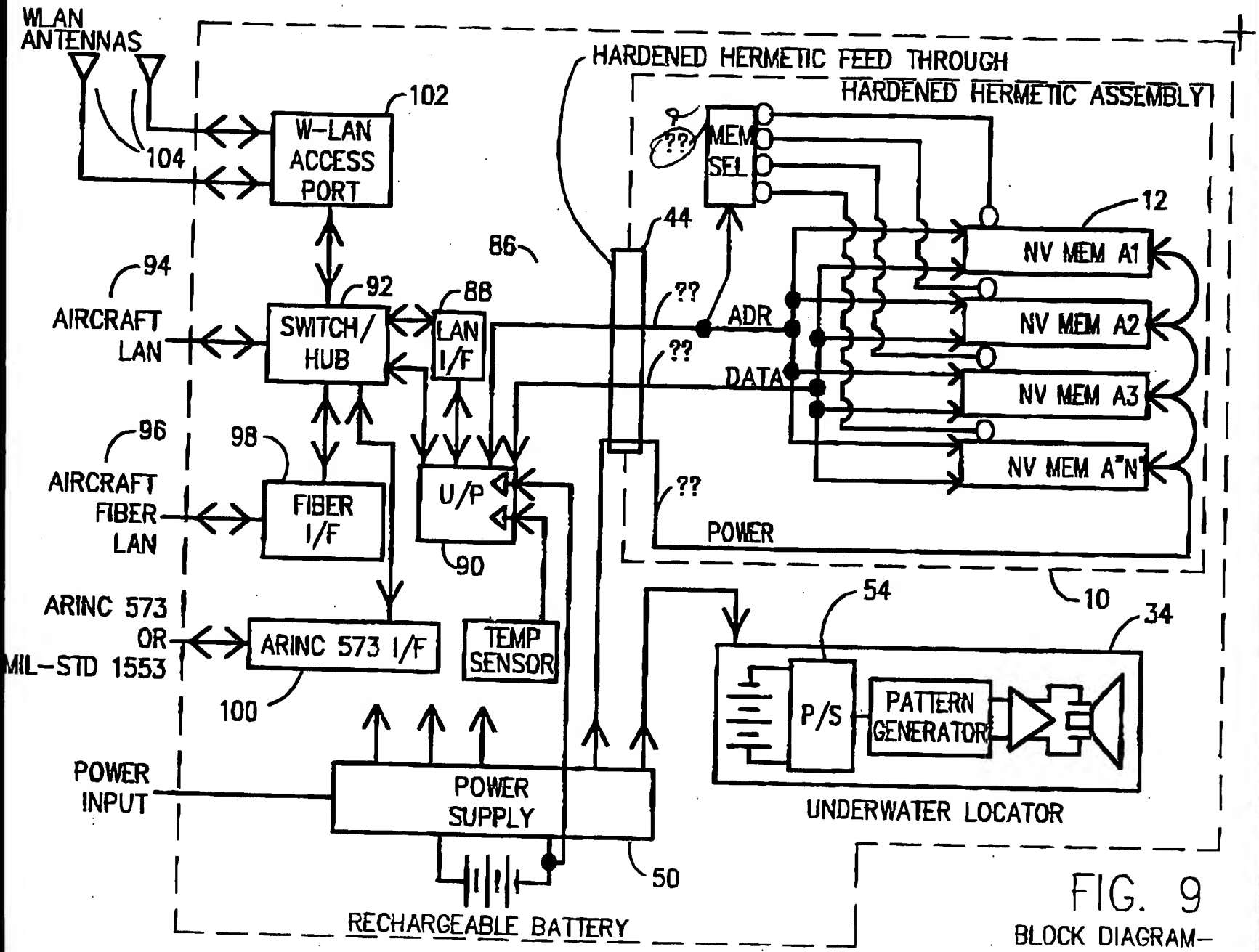


FIG. 9

BLOCK DIAGRAM–
IP LAN TO CONTROLLER

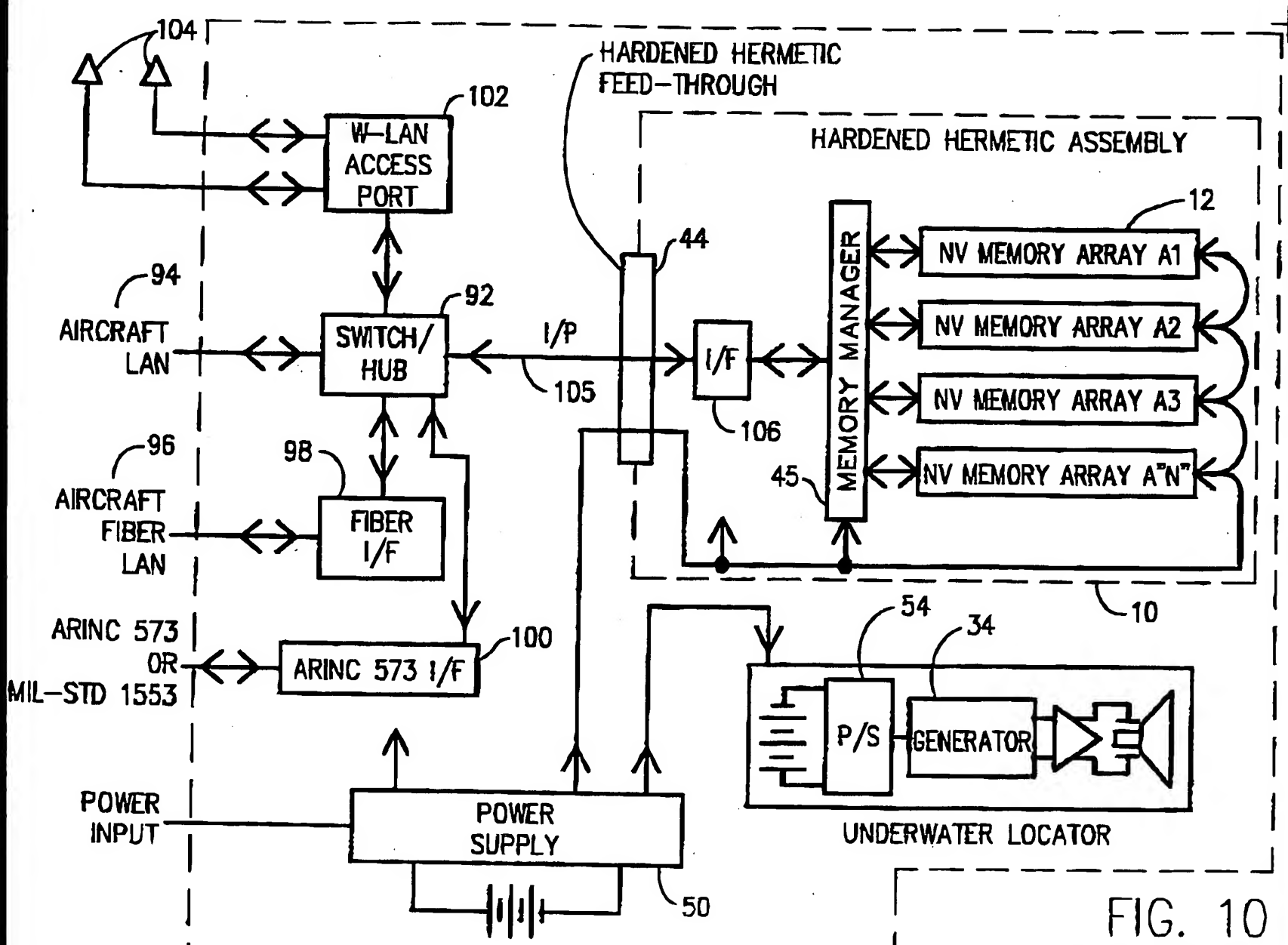


FIG. 10

BLOCK DIAGRAM-
DIRECT IP LAN TO MEMORY

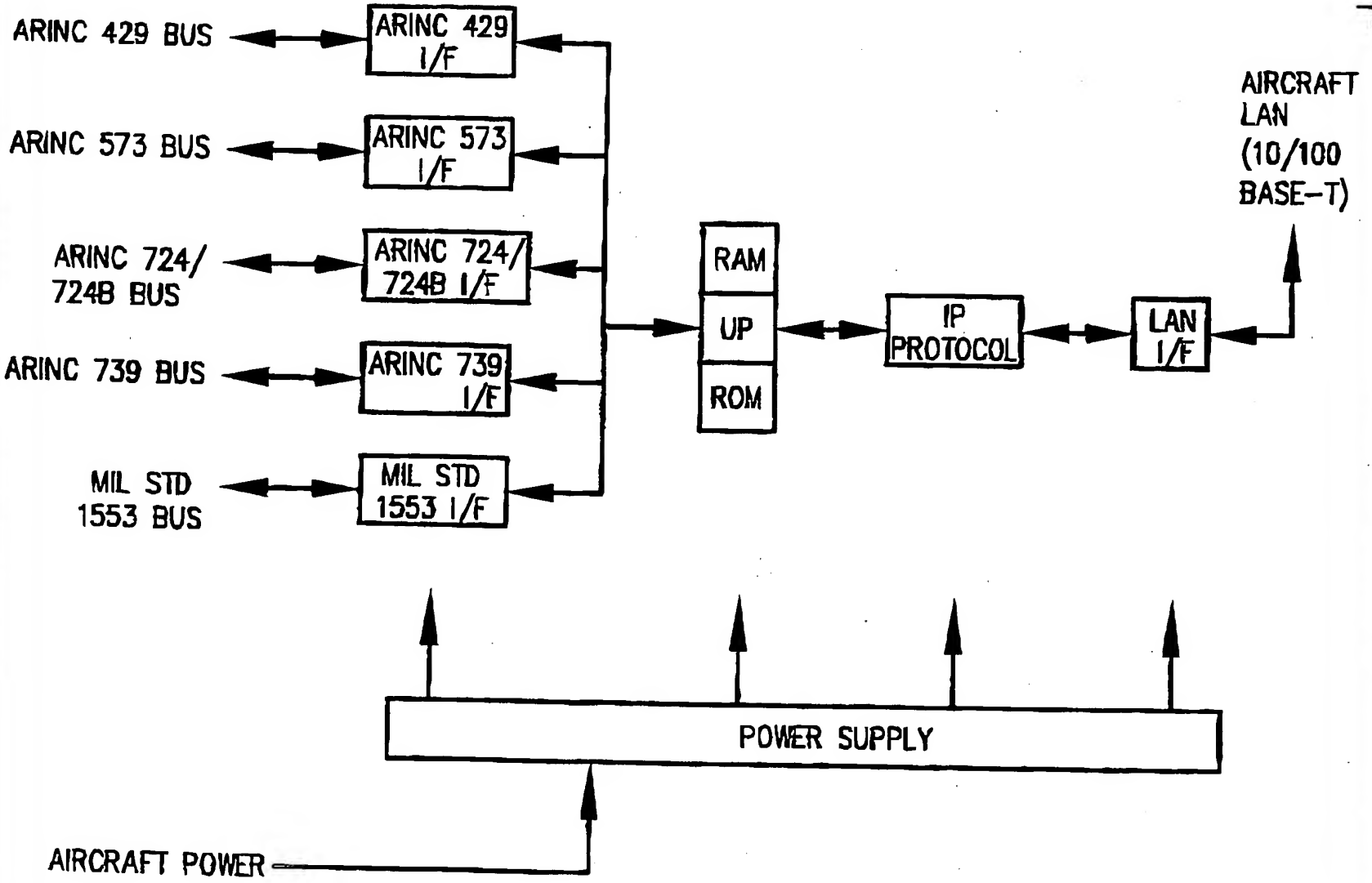


FIG. 11
PROTOCOL CONVERTER

Figs. 16A-16Z

Figs. 17A - 17M

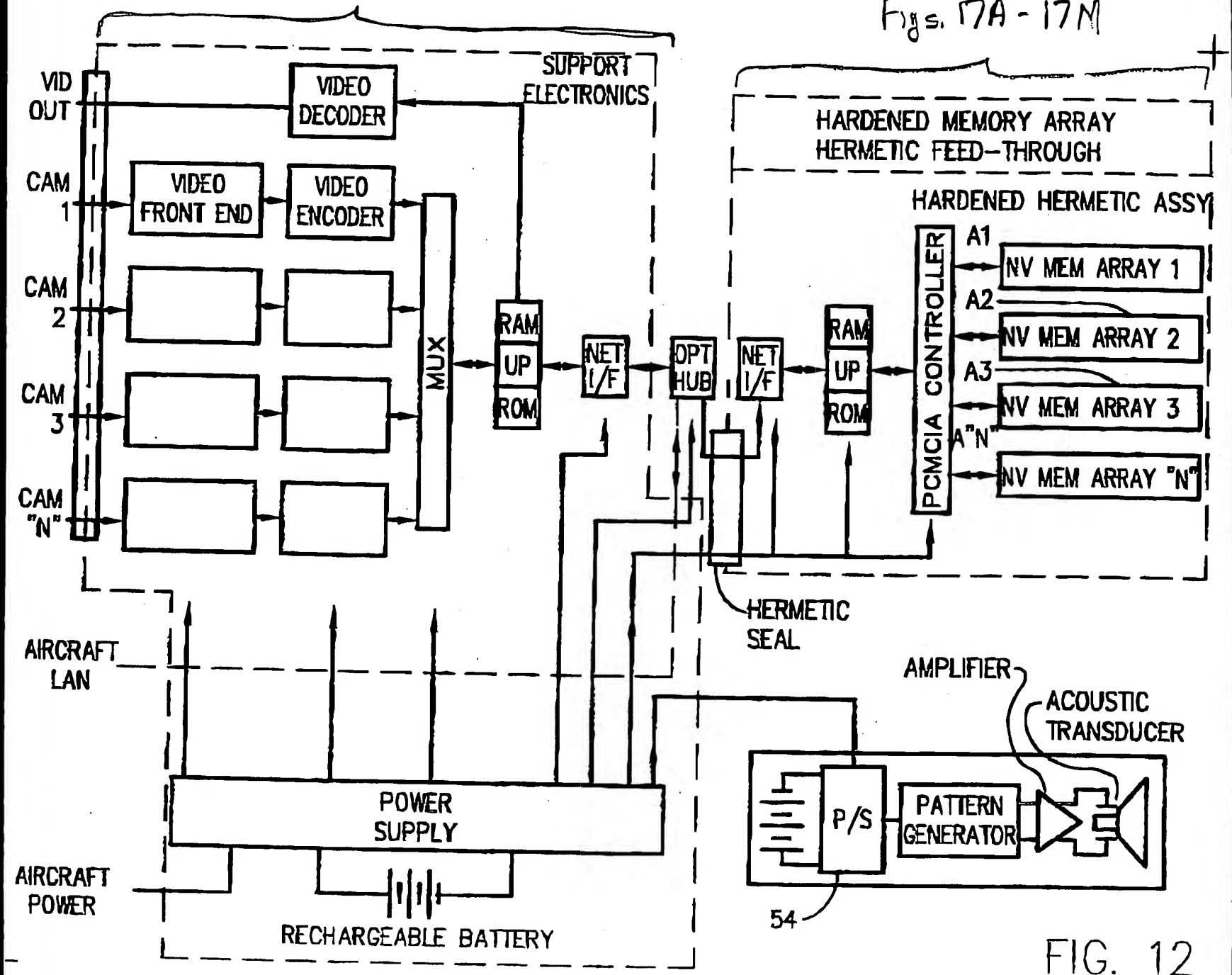
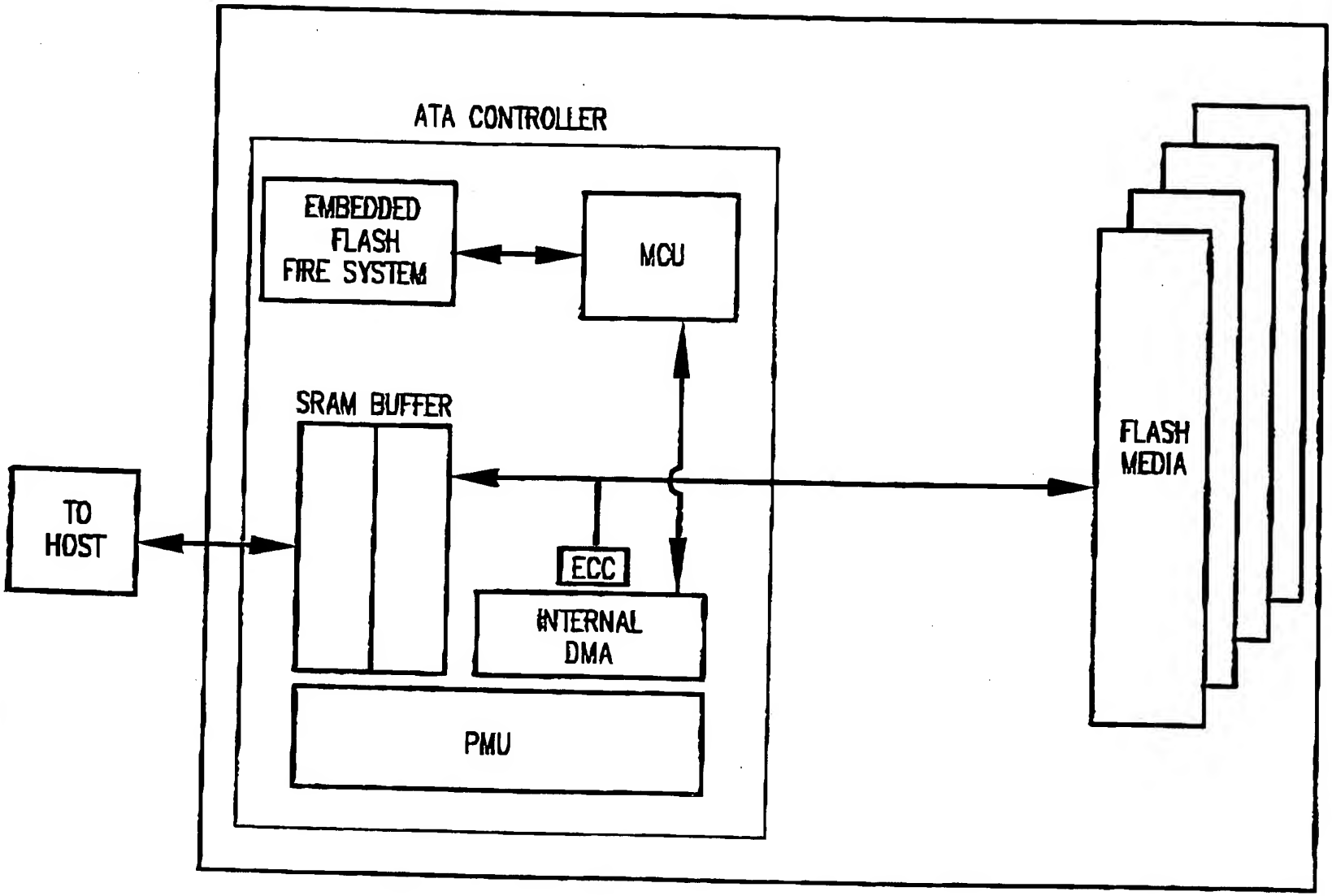


FIG. 12



SST COMPACT FLASH BLOCK DIAGRAM

FIG. 13

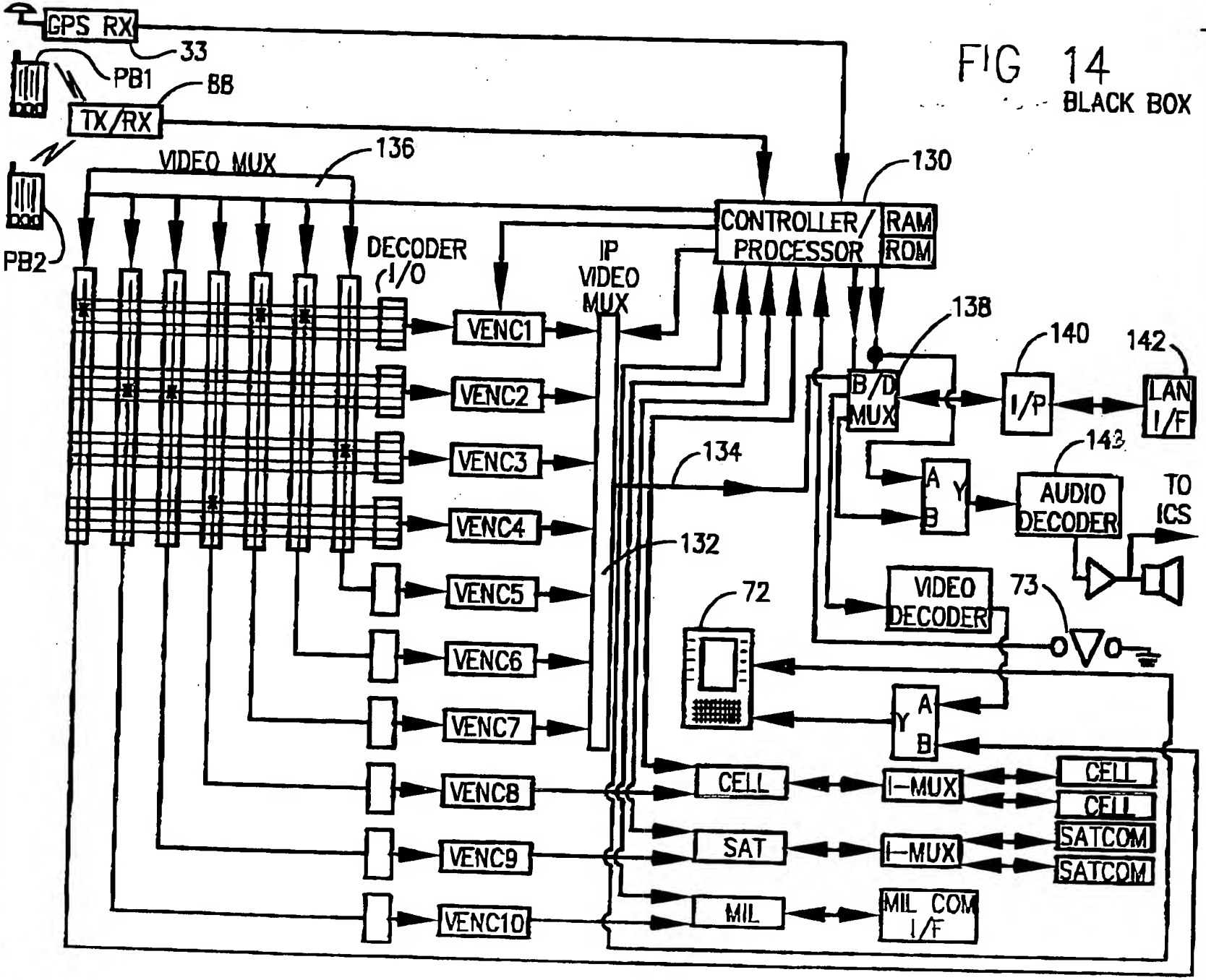


FIG 14
BLACK BOX

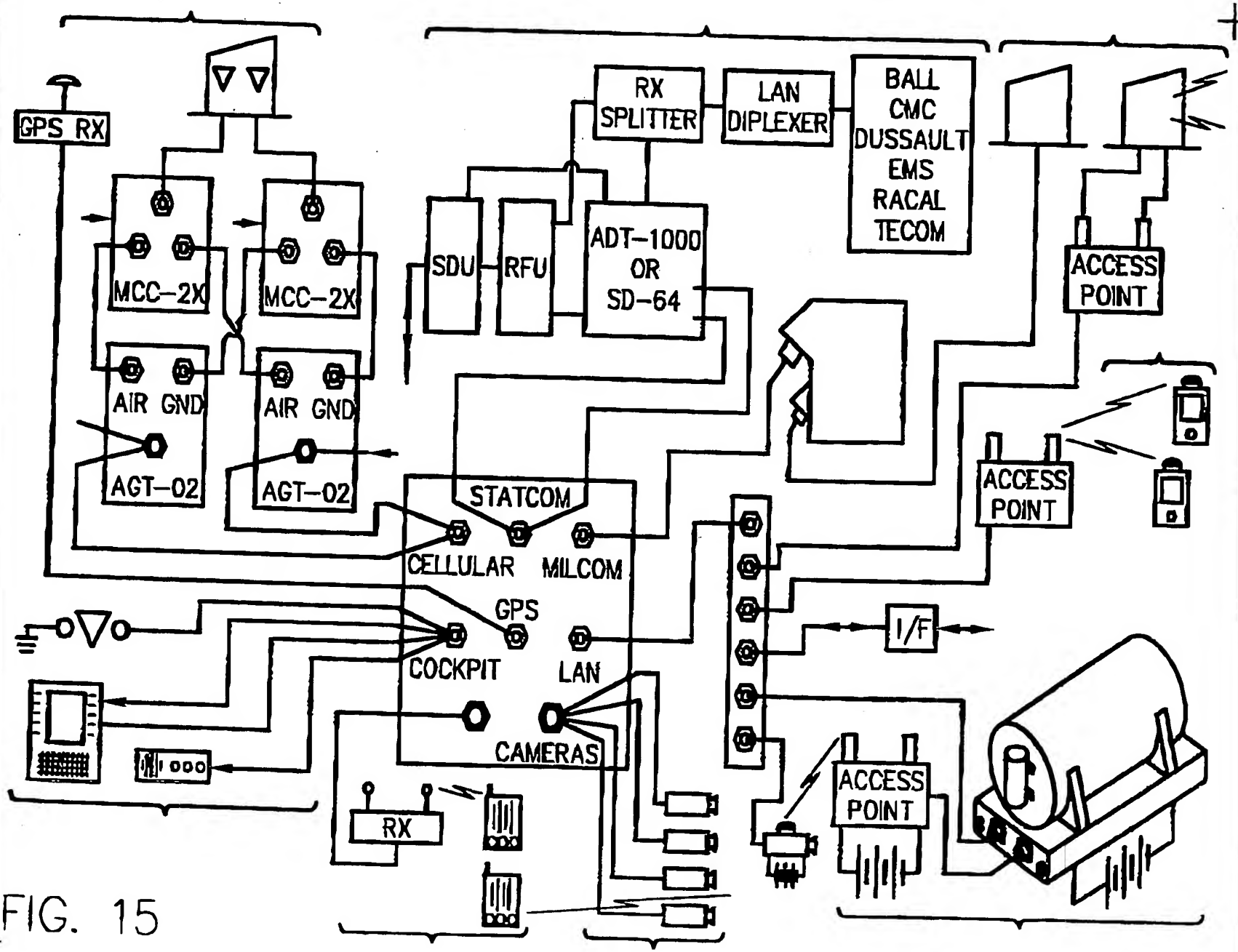
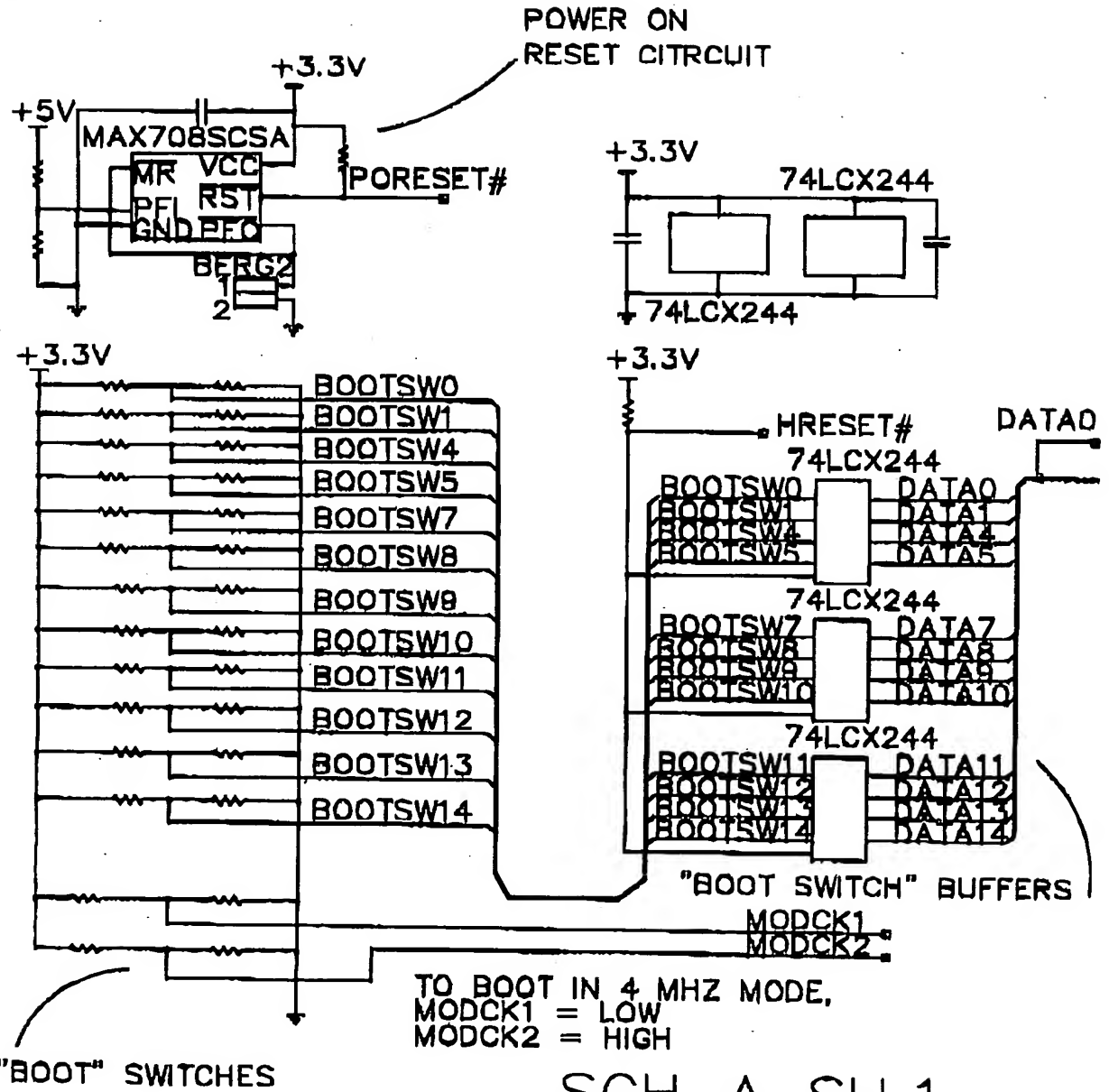

GPS RX
MCC-2X
MCC-2X
AIR GND
AIR GND
AGT-02
AGT-02
RX SPLITTER
LAN DIPLEXER
BALL
CMC
DUSSAULT
EMS
RACAL
TECOM
SDU
RFU
ADT-1000 OR SD-64
ACCESS POINT
ACCESS POINT
ACCESS POINT
STATCOM
CELLULAR
MILCOM
GPS
COCKPIT
LAN
I/F
CAMERAS
RX

FIG. 15

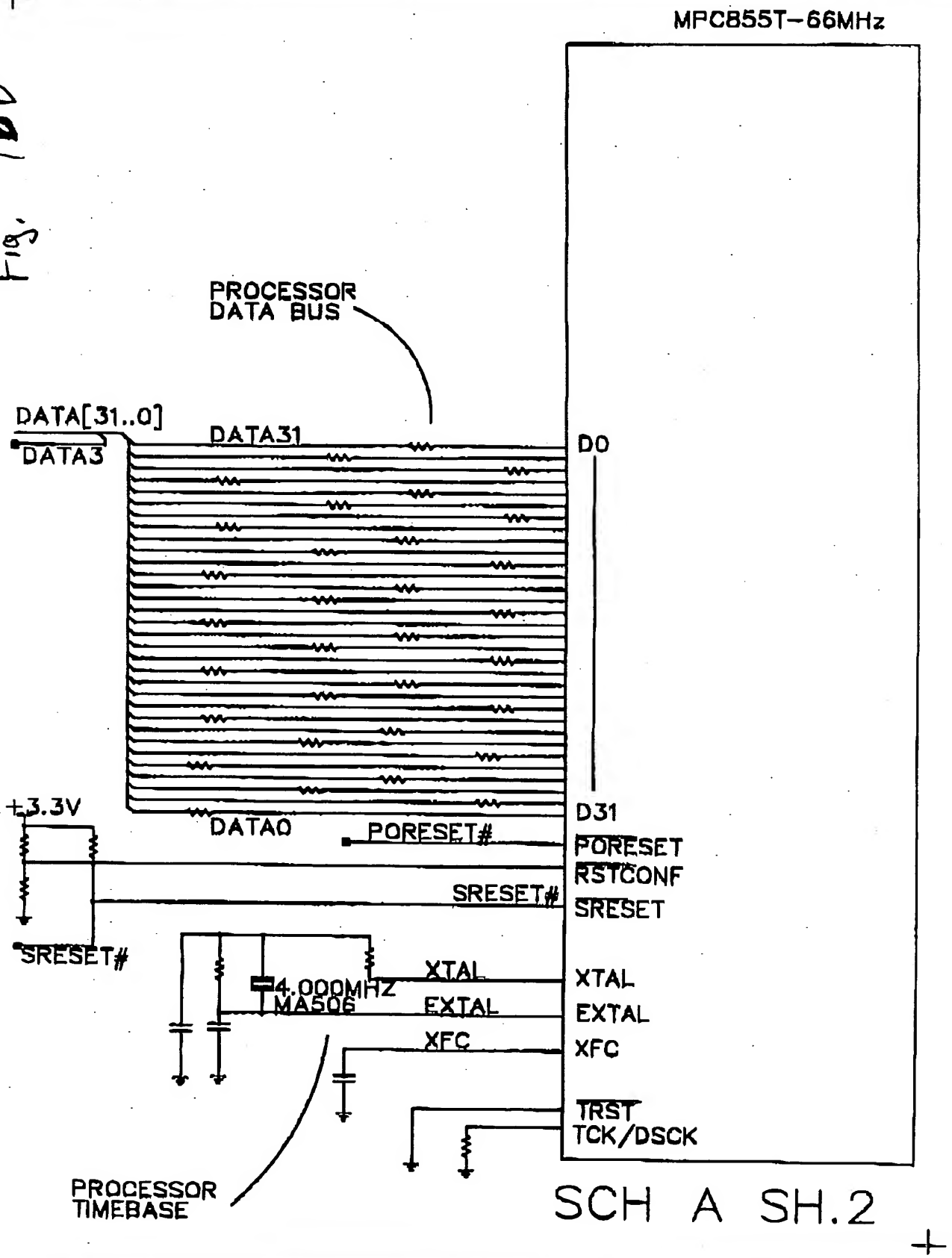
FIG 16A



SCH A SH.1

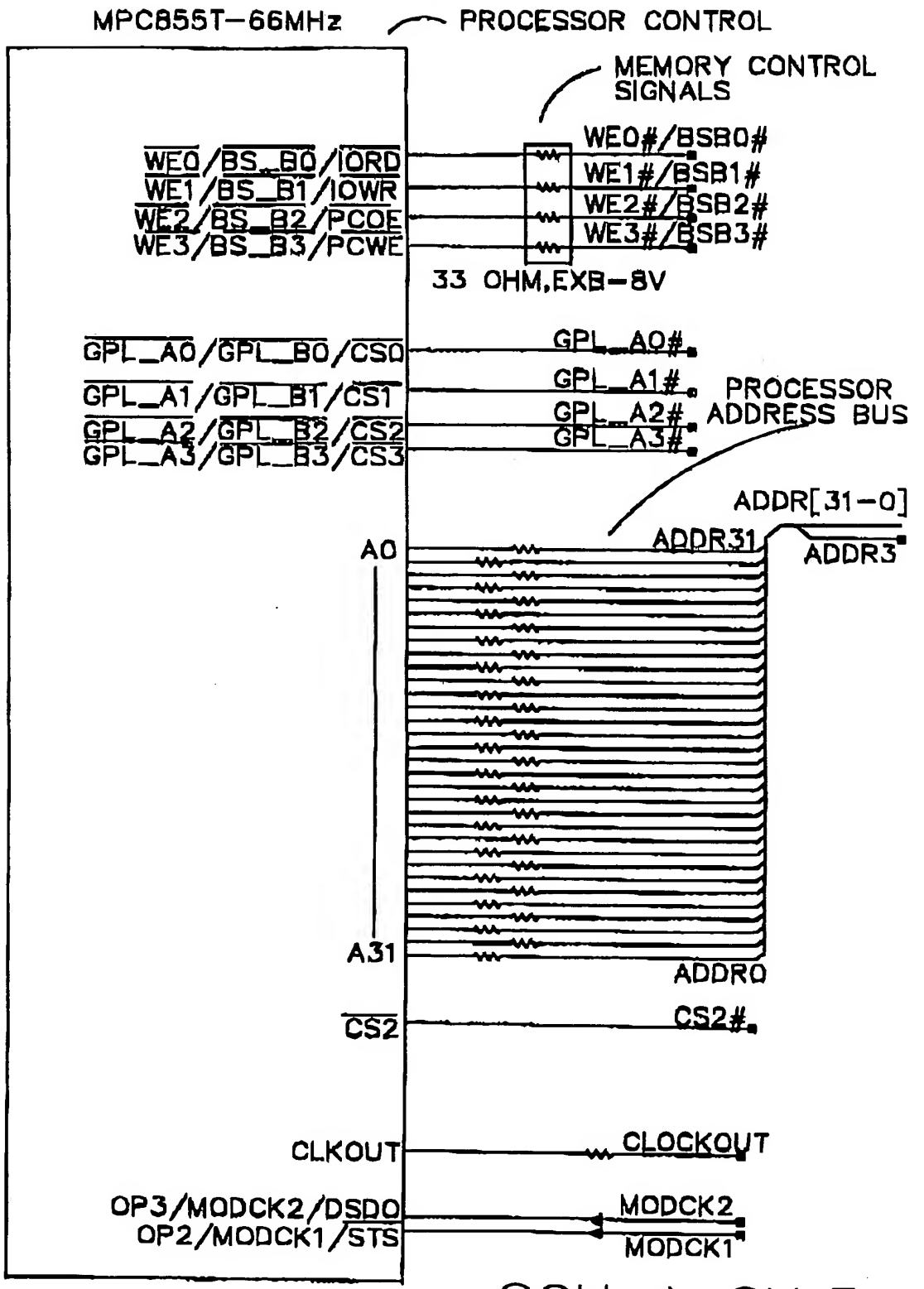
LOGIC POWER BOOT PROCESSOR MEMORY ARRAY

Fig. 16b



Motorola MPC855T Processor Data Bus

Fig. 16C



SCH A SH.3

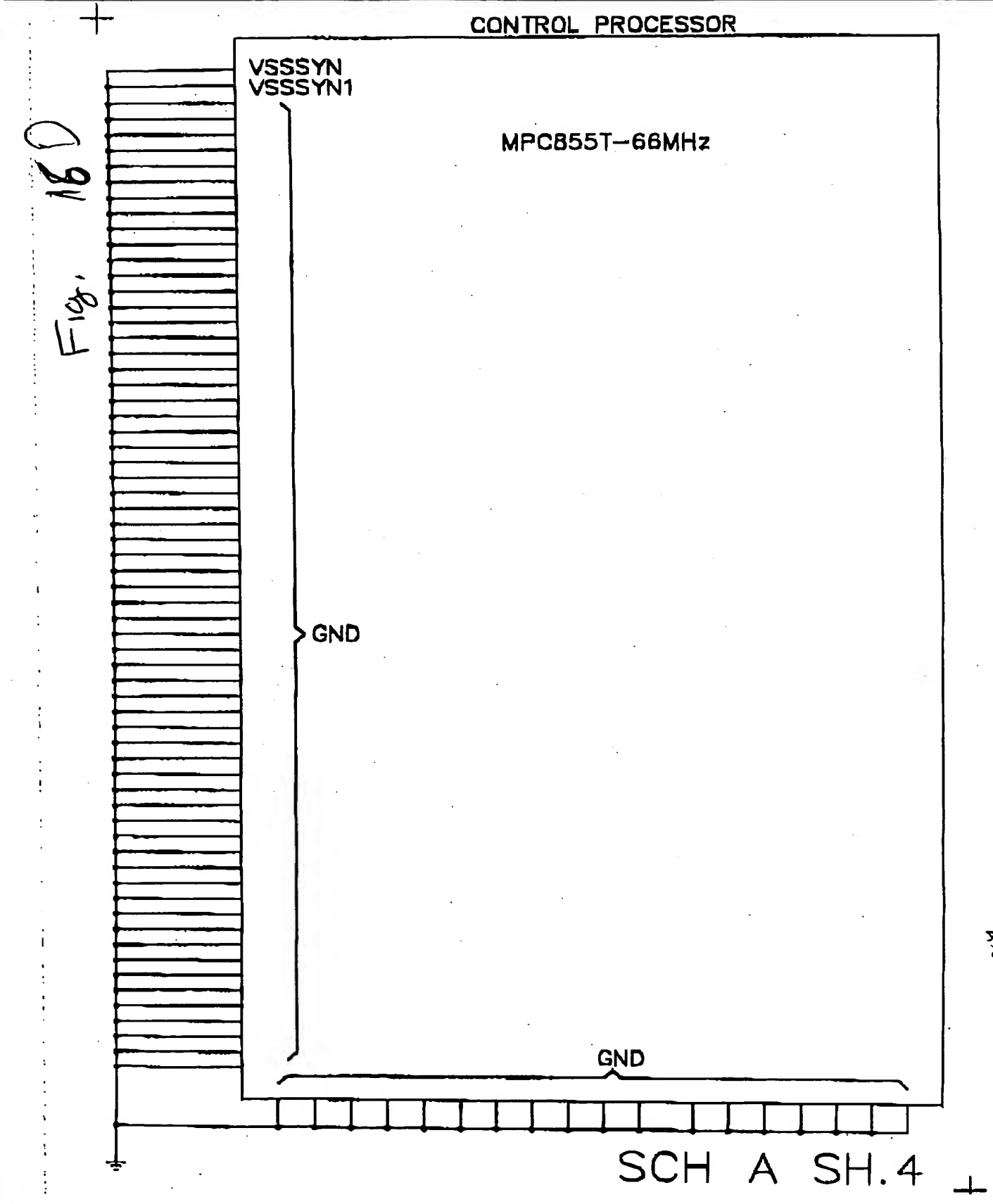


Fig. 16D

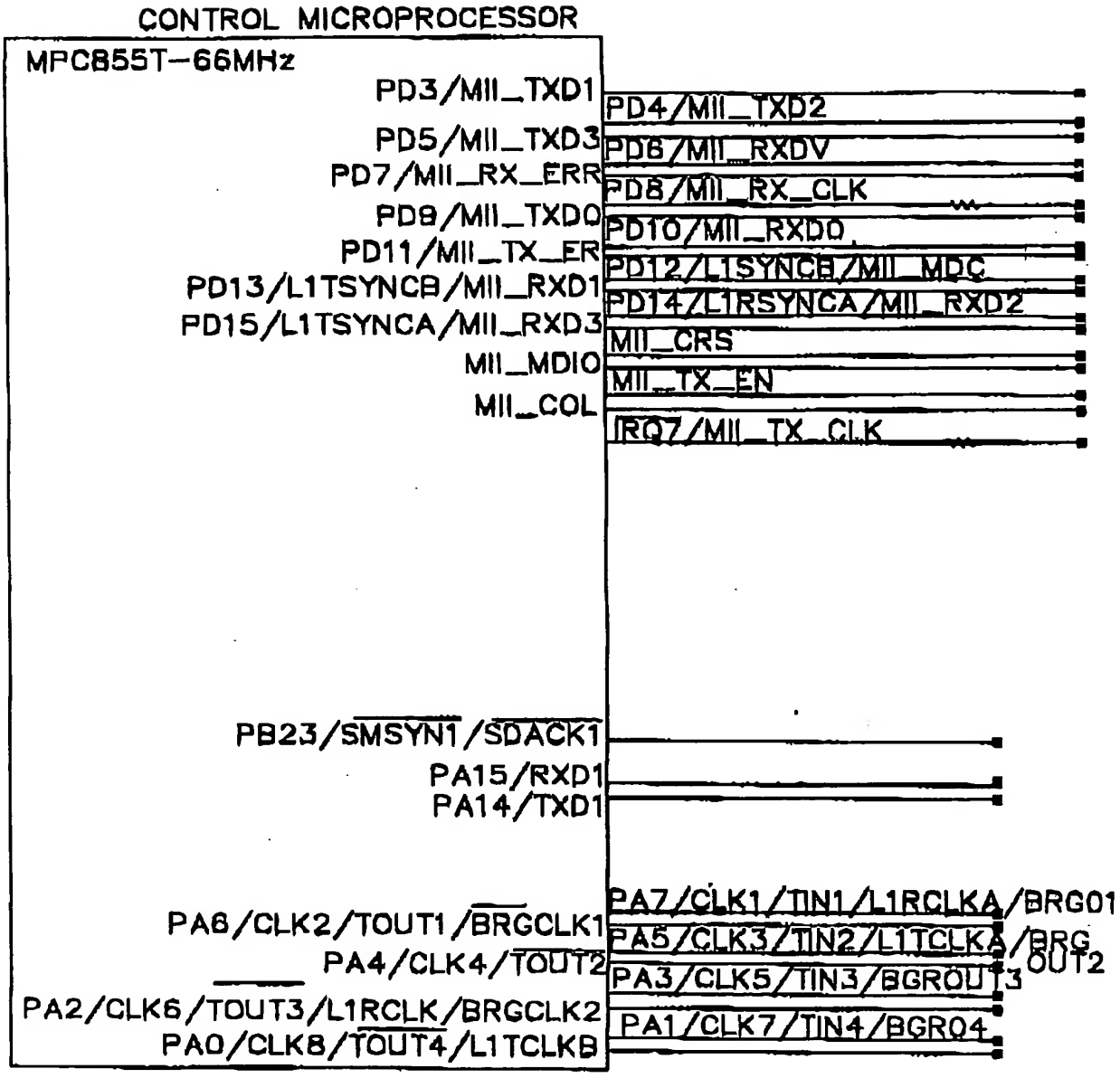
Memory Array Processor Grounds

391

Fig

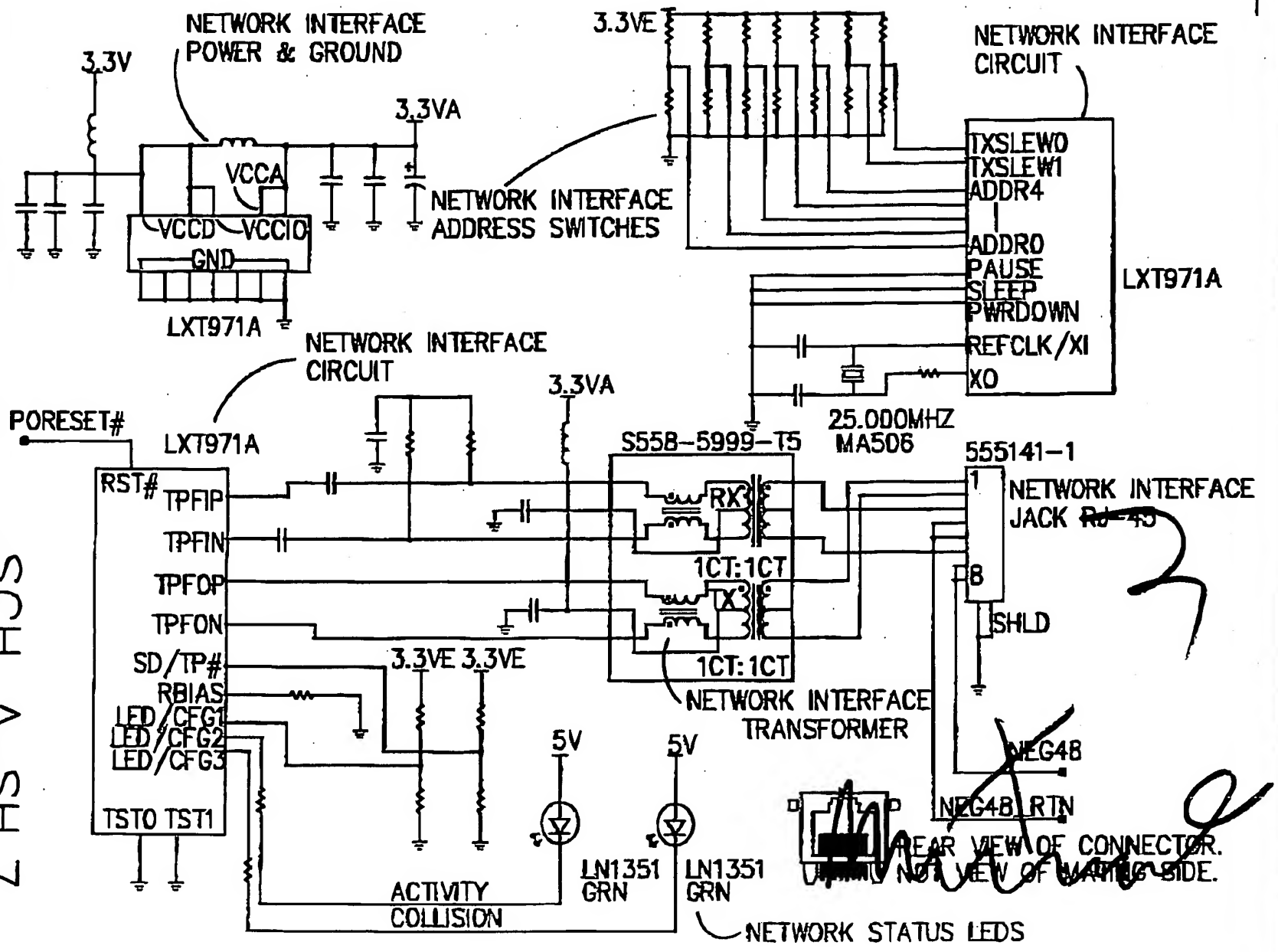
SCH A SH.5

Fig 9-1



SCH A SH.6

Fig 16G



SCH A SH 7

MEMORY ARRAY | LAN INTERFACE AND POWER TAP

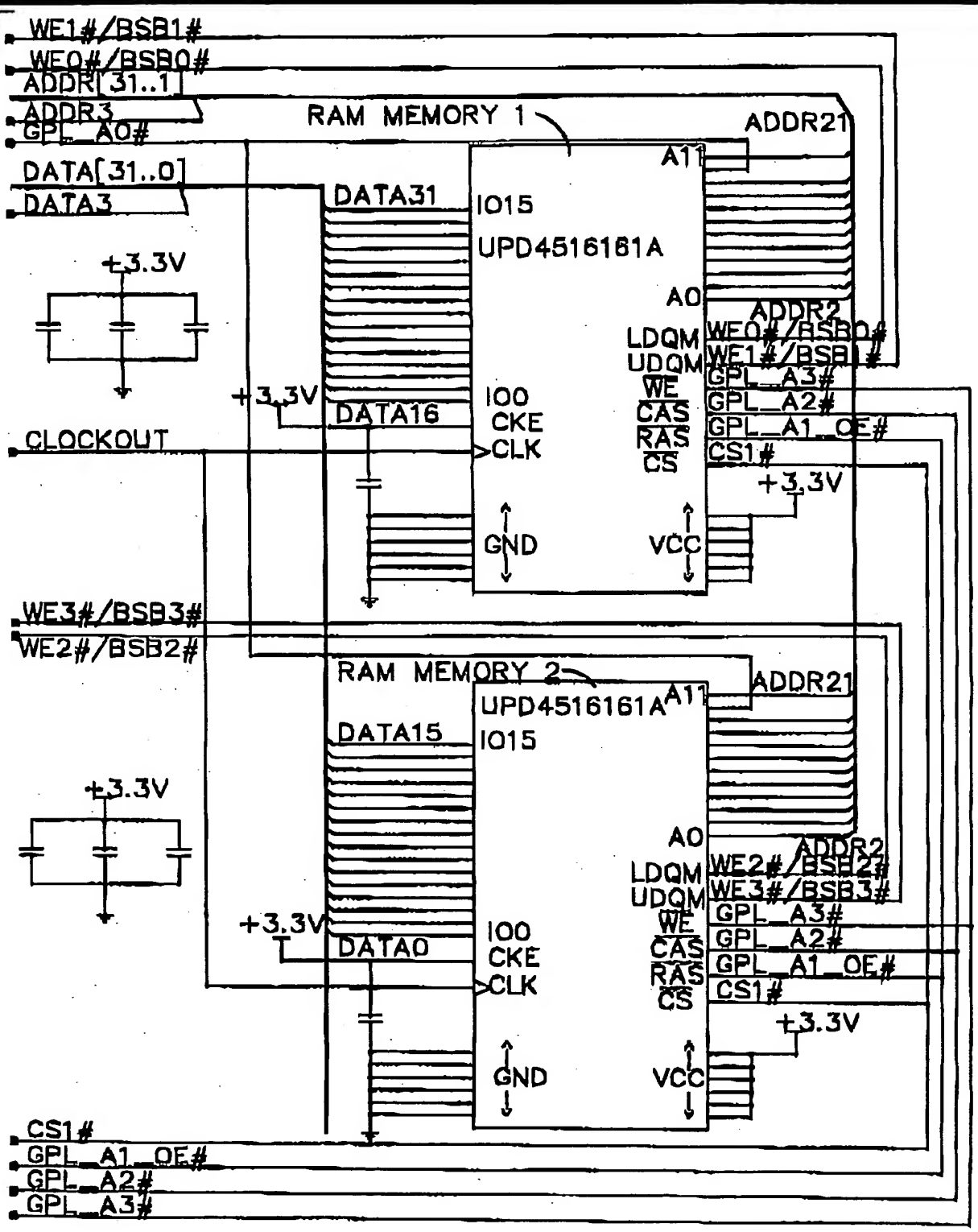
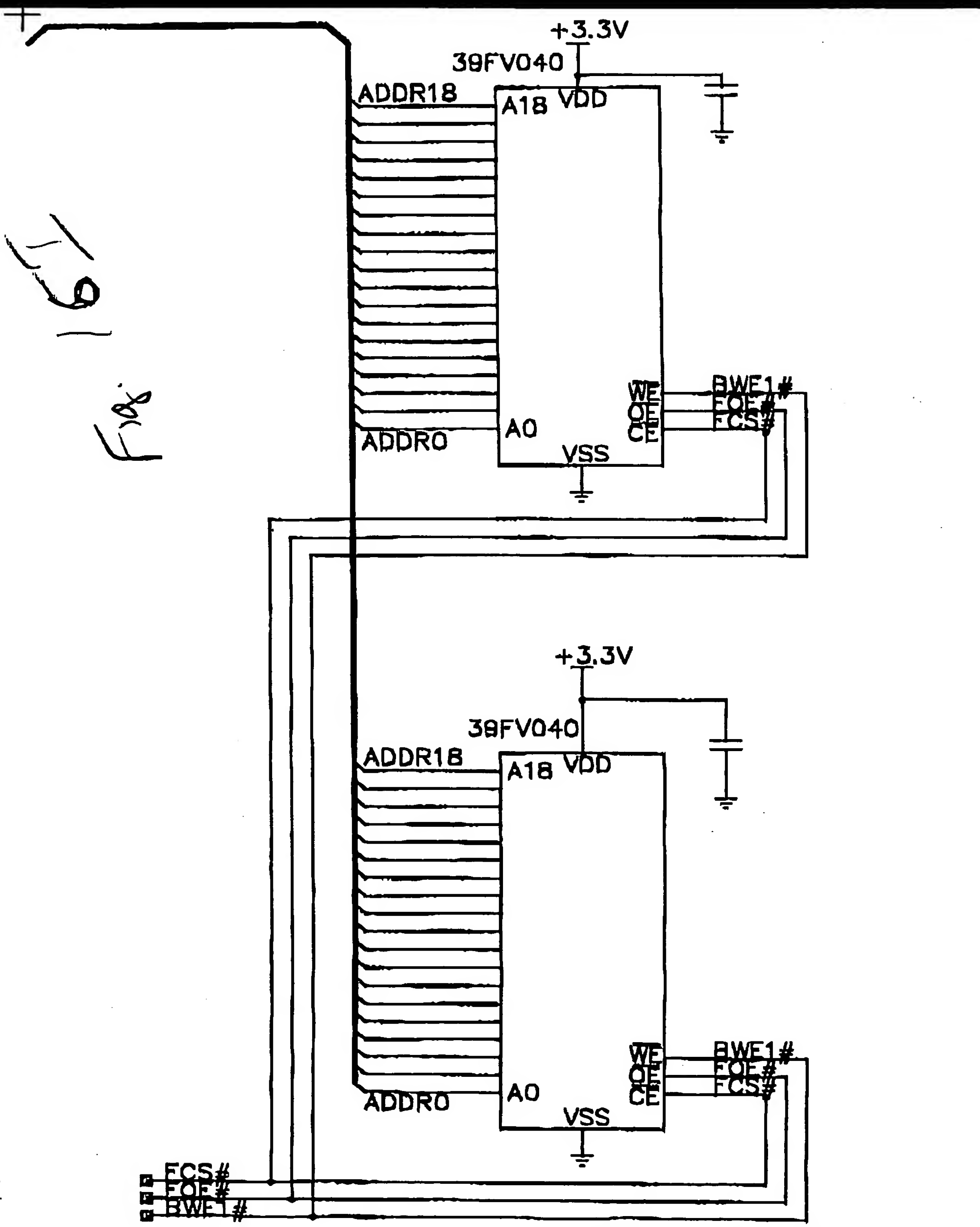


FIG 16H

SCH A SH.8

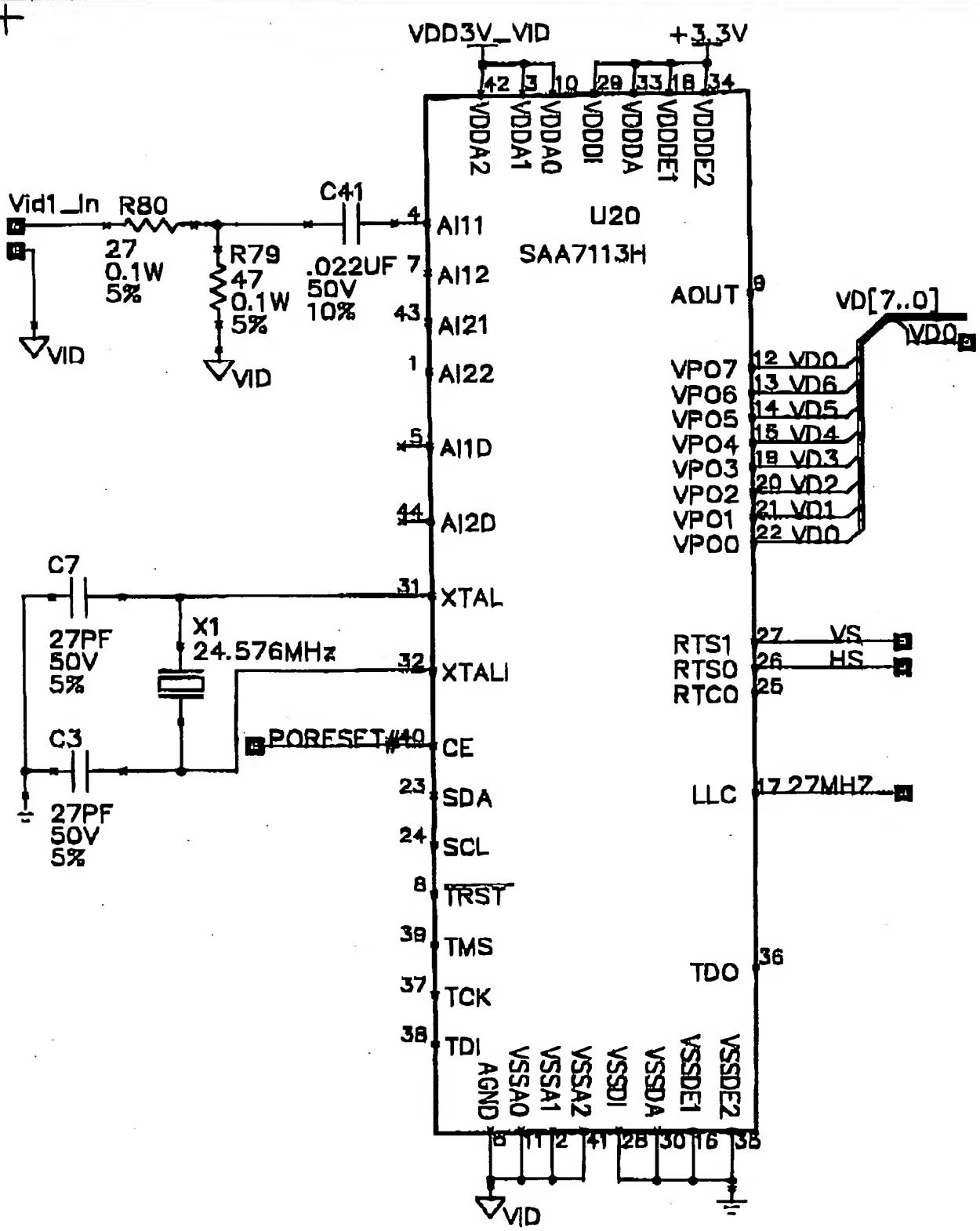
Fig. 16



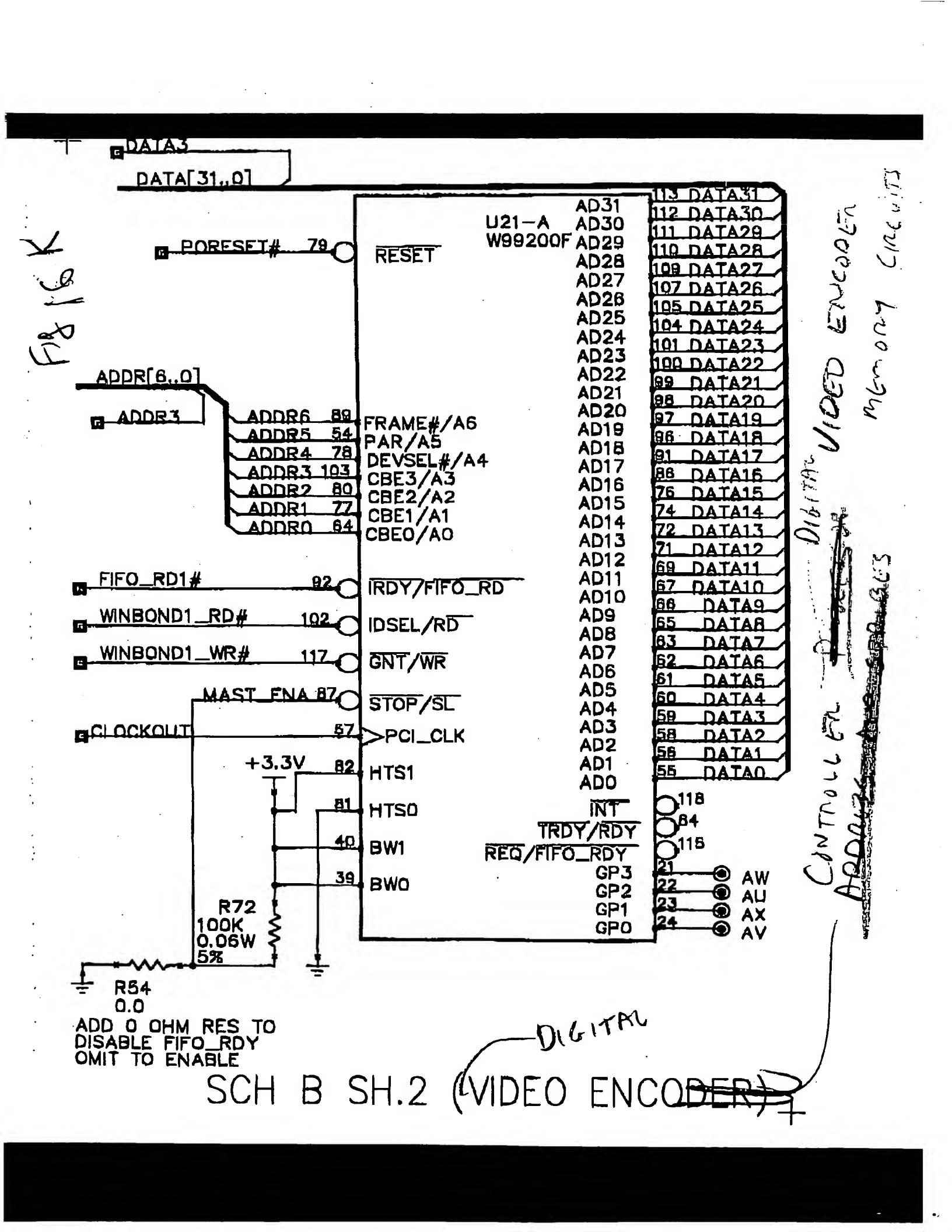
SCH A SH.9

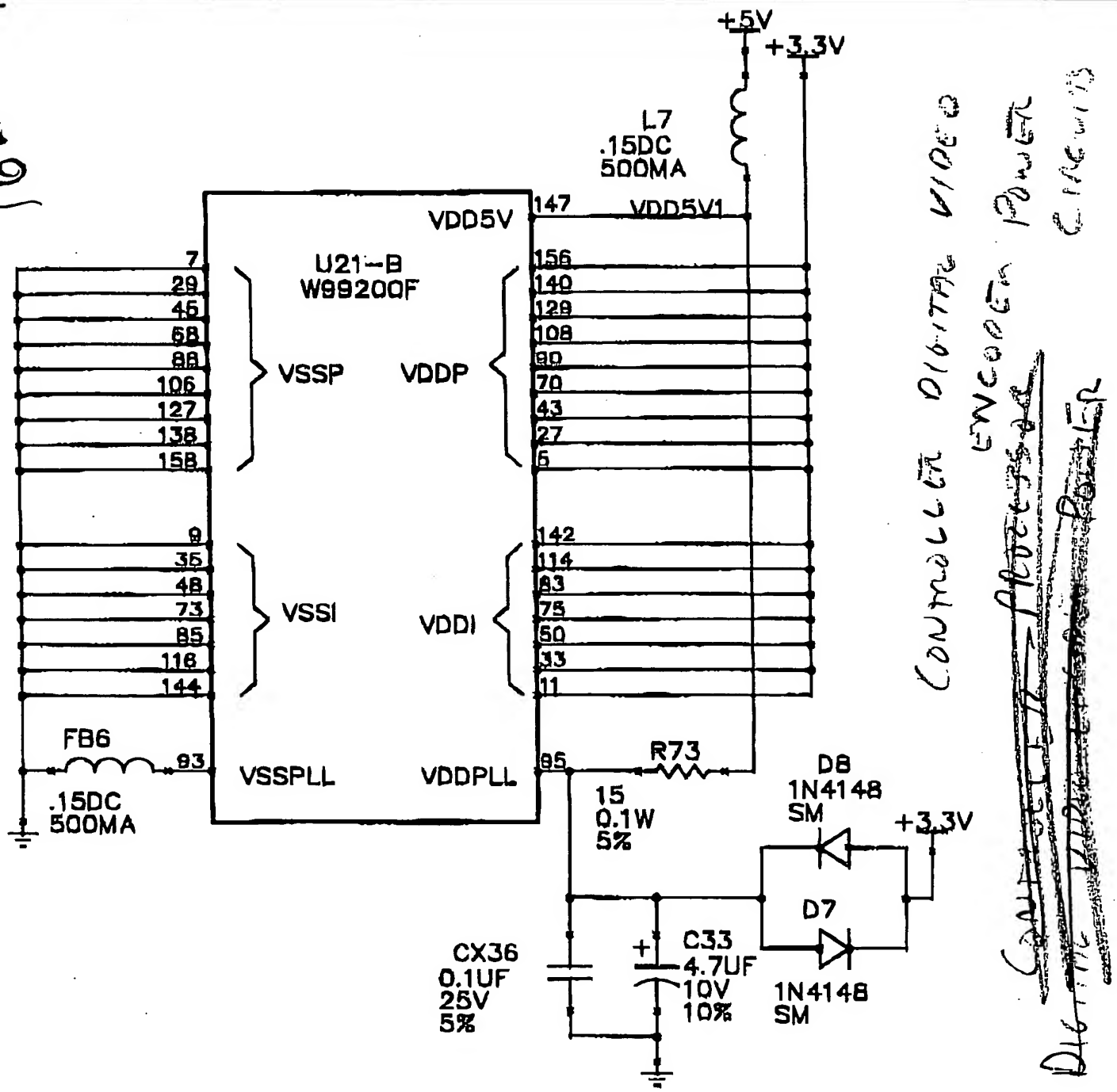
Non-volatile memory

Memory and processor

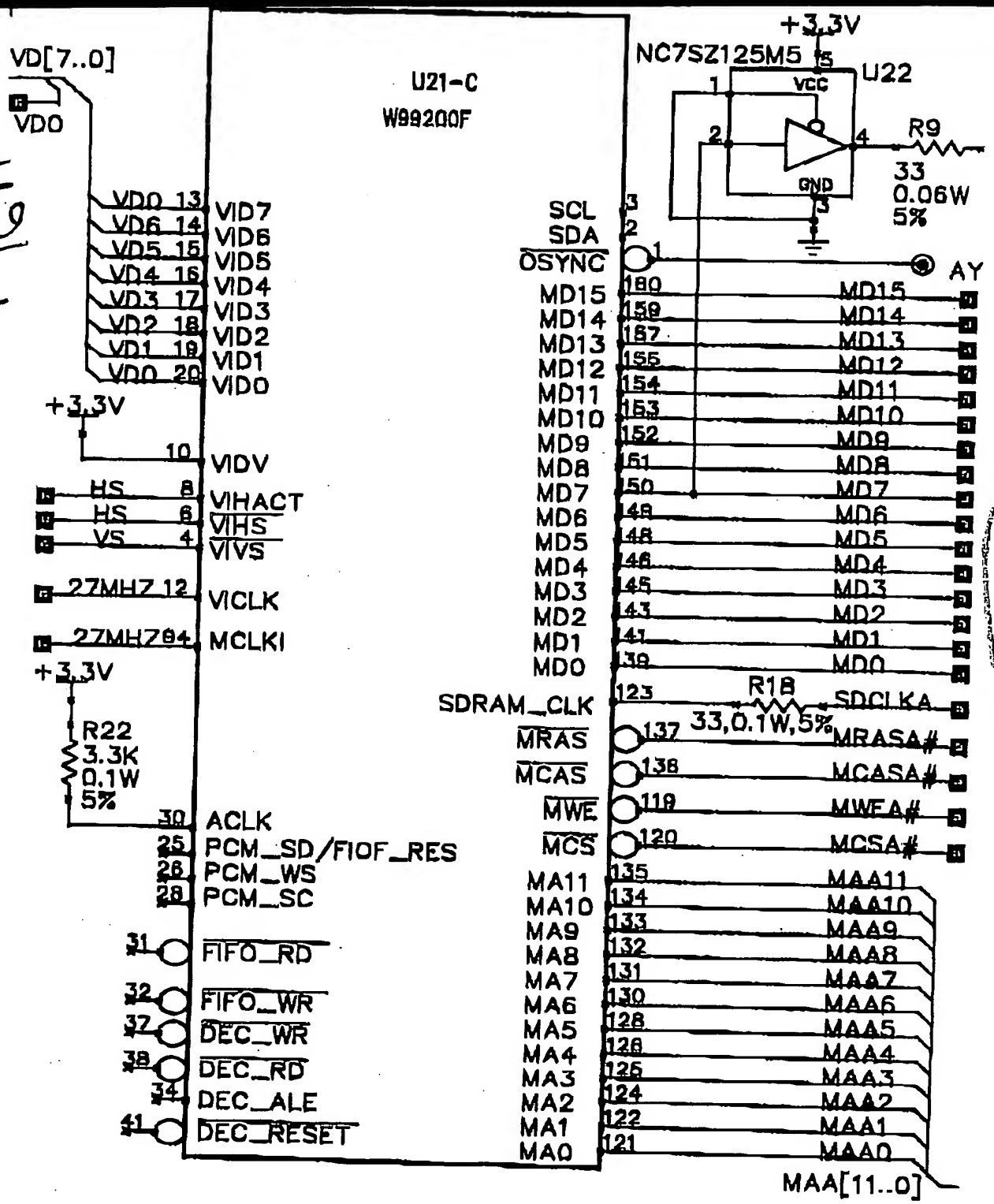


SCH B SH.1 (VIDEO FRONT END)

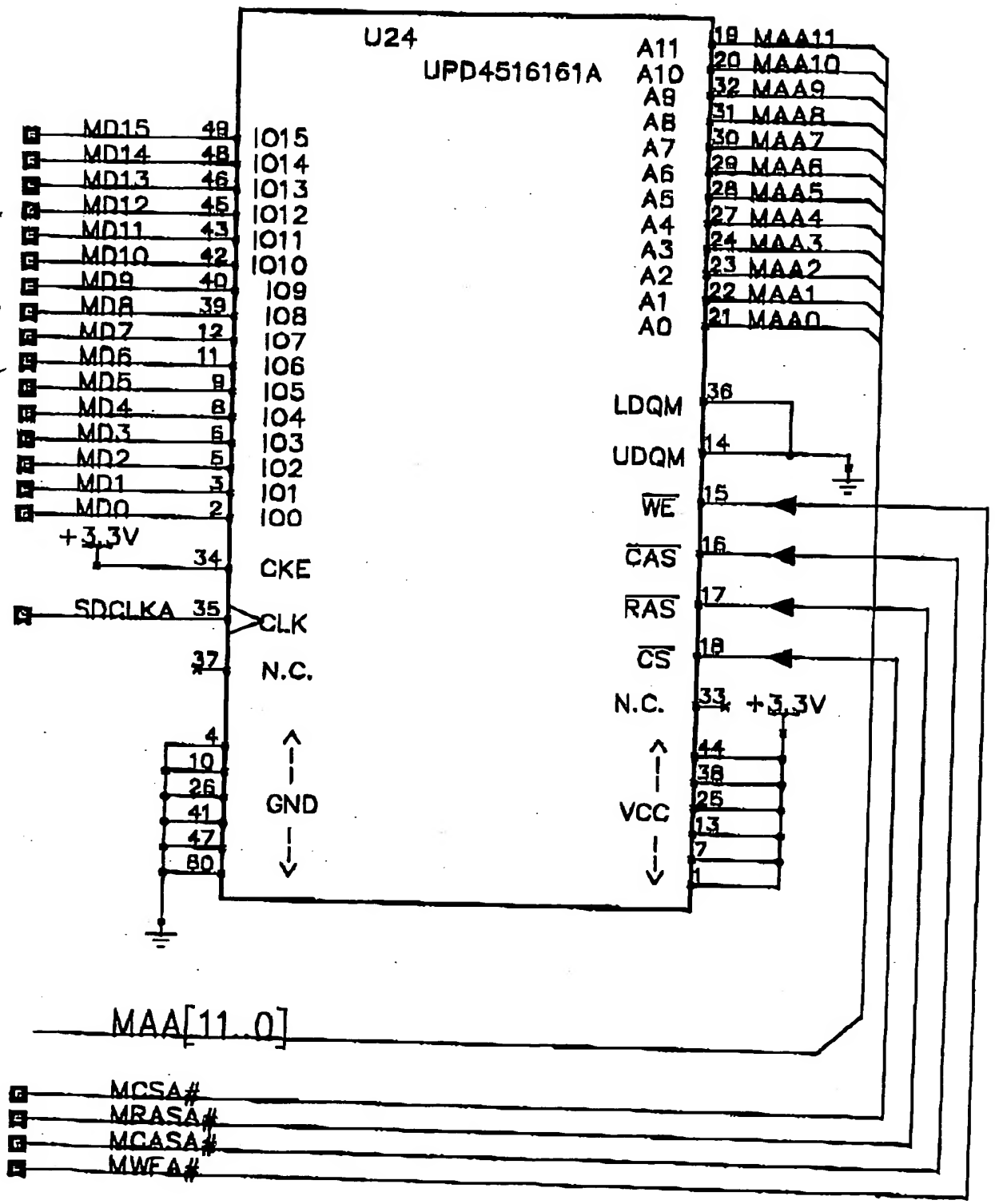

DATA3
DATA[31..0]
U21-A
W99200F
PORESET# 79
RESET
ADDR[6..0]
ADDR3
ADDR6 88 FRAME#/A6
ADDR5 54 PAR/A5
ADDR4 78 DEVSEL#/A4
ADDR3 103 CBE3/A3
ADDR2 80 CBE2/A2
ADDR1 77 CBE1/A1
ADDR0 64 CBE0/A0
FIFO_RD1# 92 IRDY/FIFO_RD
WINBOND1_RD# 102 IDSEL/RD
WINBOND1_WR# 117 GNT/WR
MAST_ENA 87 STOP/SL
CLOCKOUT 57 PCI_CLK
+3.3V
82 HTS1
81 HTS0
40 BW1
39 BW0
R72
100K
0.06W
5%
R54
0.0
ADD 0 OHM RES TO
DISABLE FIFO_RDY
OMIT TO ENABLE
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
INT 118
TRDY/RDY 84
REQ/FIFO_RDY 115
GP3 21 AW
GP2 22 AU
GP1 23 AX
GP0 24 AV
113 DATA31
112 DATA30
111 DATA29
110 DATA28
109 DATA27
107 DATA26
105 DATA25
104 DATA24
101 DATA23
100 DATA22
99 DATA21
98 DATA20
97 DATA19
96 DATA18
91 DATA17
86 DATA16
76 DATA15
74 DATA14
72 DATA13
71 DATA12
69 DATA11
67 DATA10
66 DATA9
65 DATA8
63 DATA7
62 DATA6
61 DATA5
60 DATA4
59 DATA3
58 DATA2
56 DATA1
55 DATA0
DIGITAL VIDEO ENCODER
CONTROLLER
DIGITAL
SCH B SH.2 (VIDEO ENCODER)



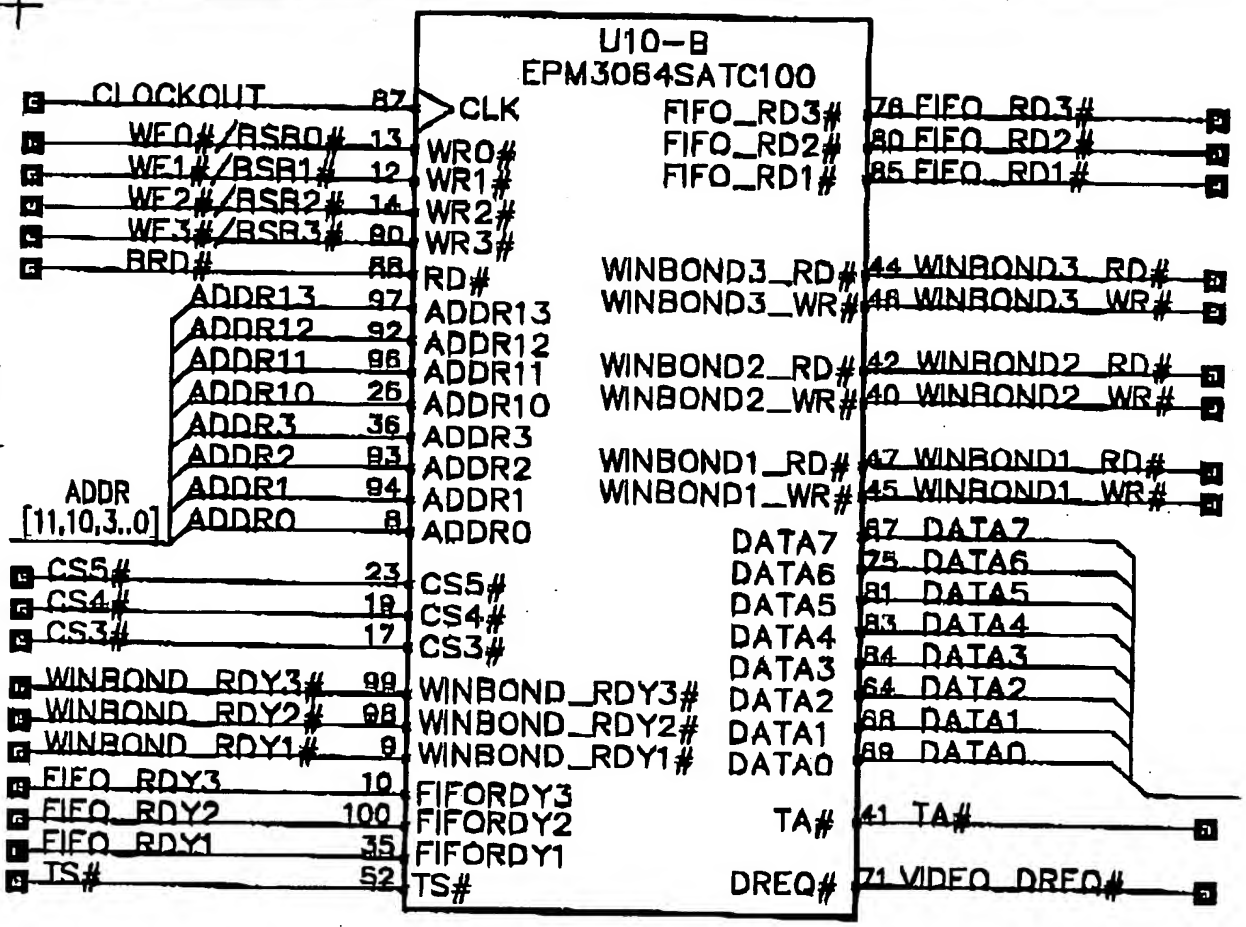
SCH B SH.3 (VIDEO ENCODER)

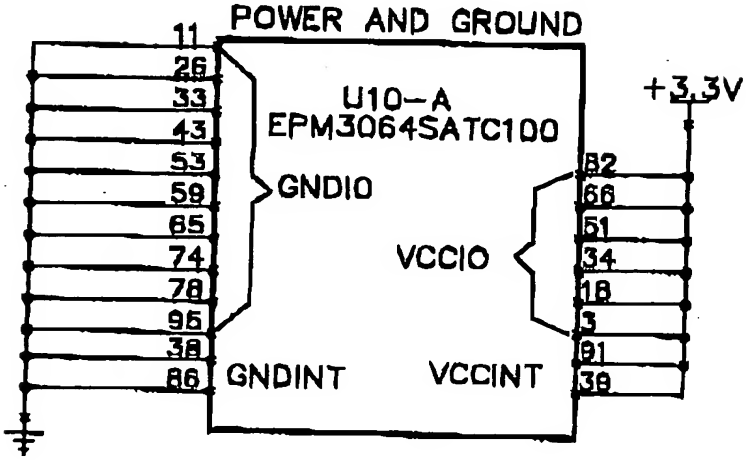


SCH B SH.4 (VIDEO ENCODER)



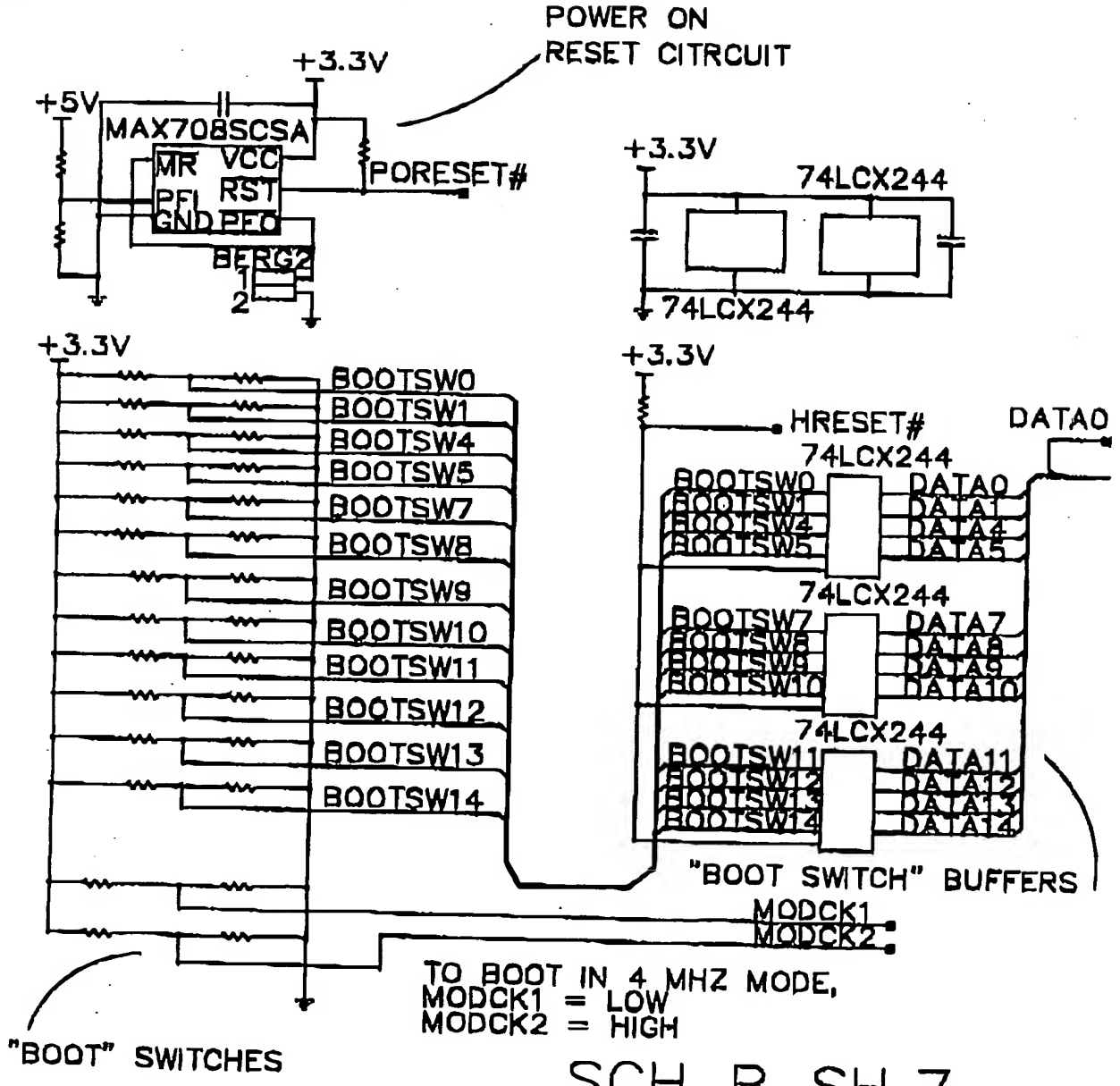
SCH B SH.5 (VIDEO ENCODER)





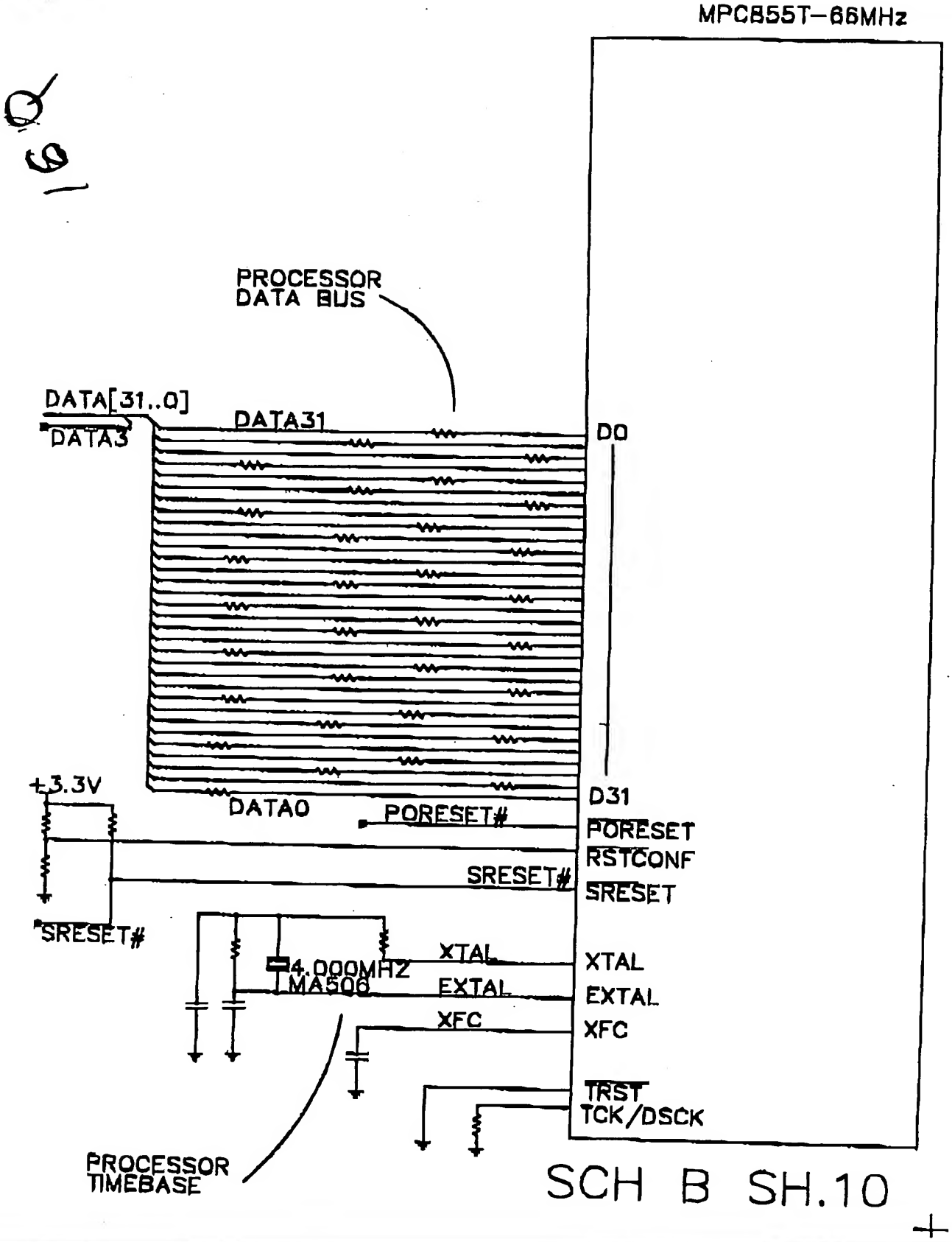
SCH B SH.6 (VIDEO ENCODER)

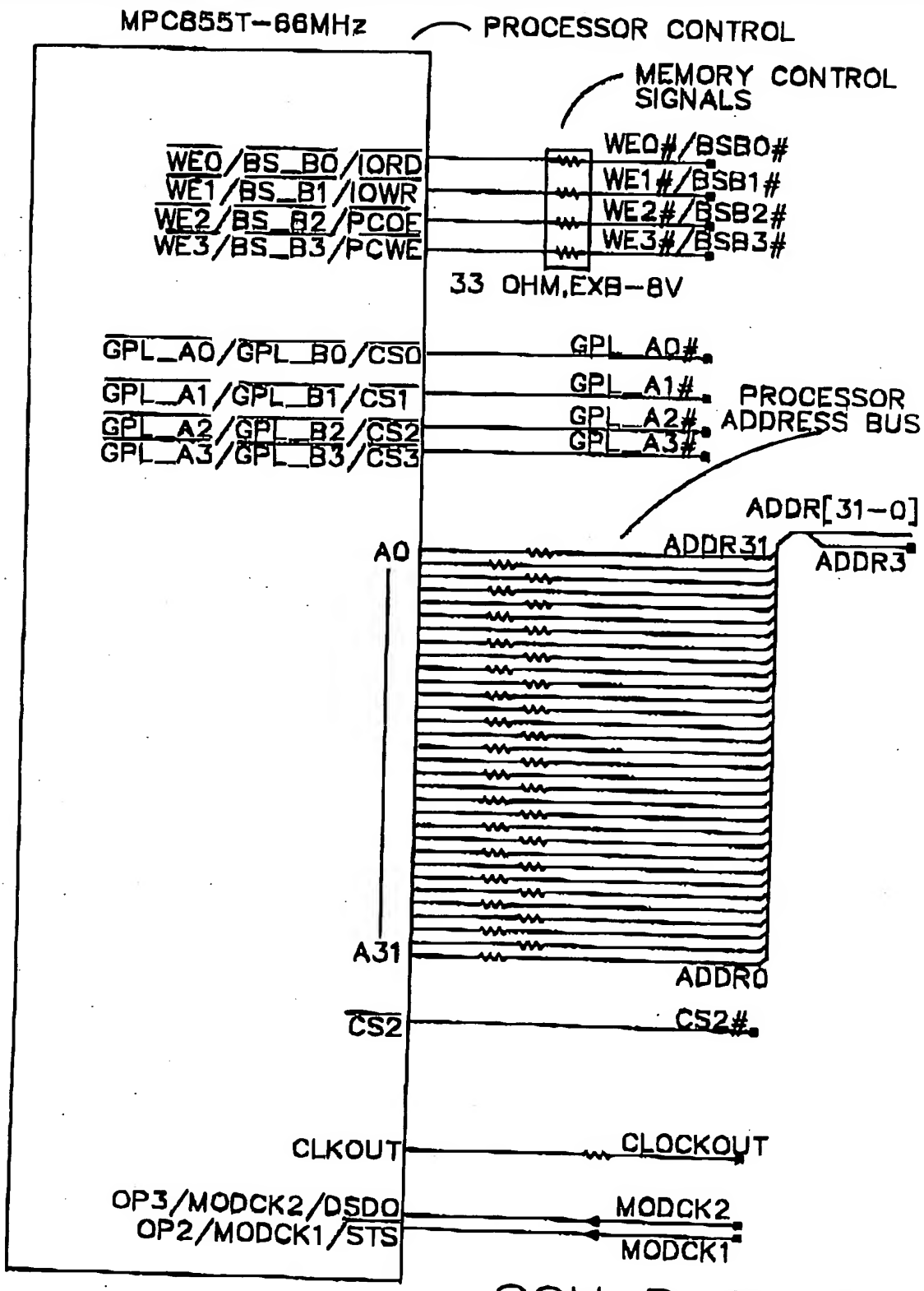
FIG 8
1



SCH B SH.7

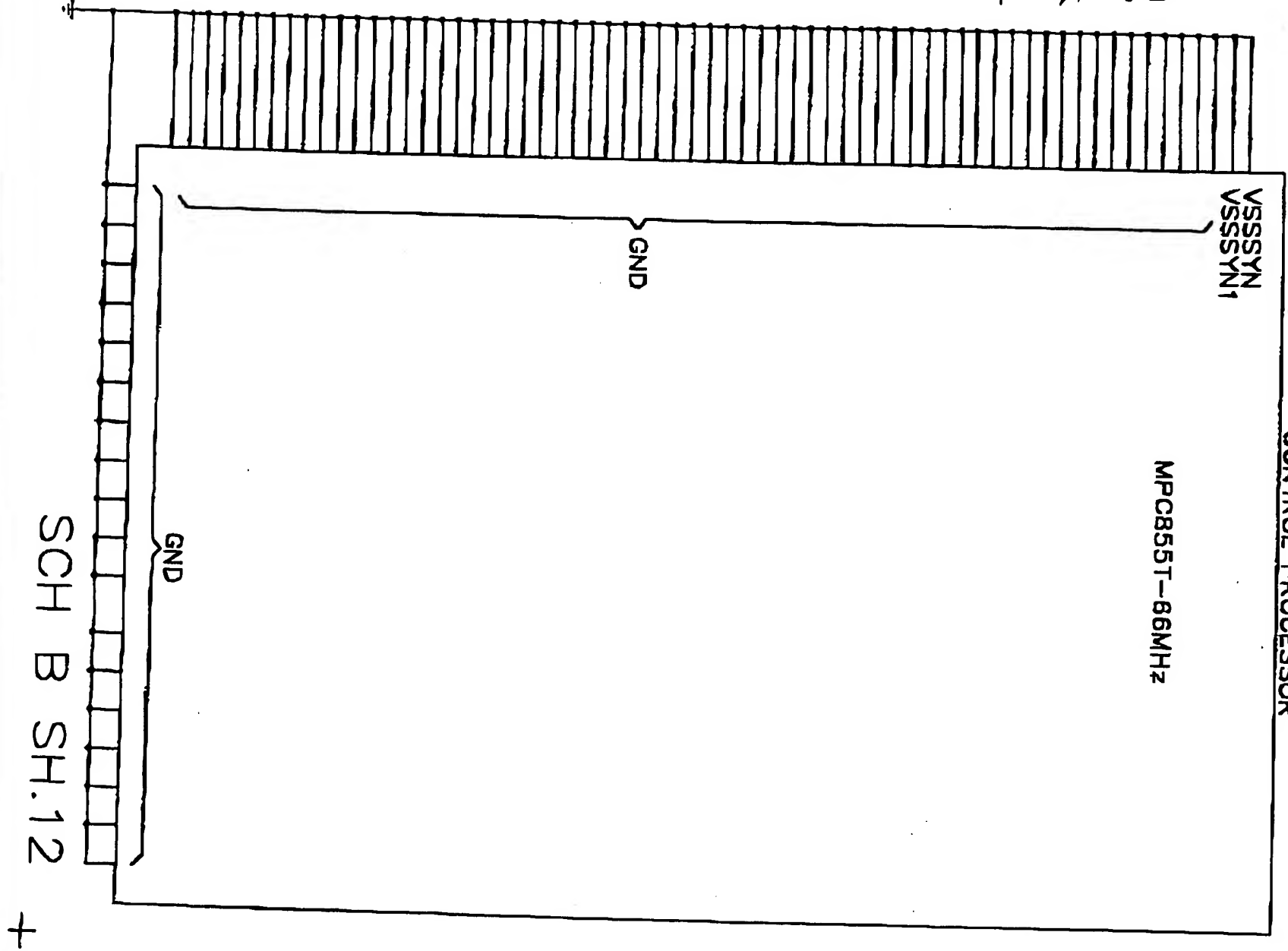
CAN MODULE PROCESSOR BOOT LOGIC


MPC855T–66MHz
PROCESSOR
DATA BUS
DATA[31..0]
DATA31
DATA3
DATA0
D0
D31
+3.3V
PORESET#
PORESET
RSTCONF
SRESET#
SRESET
SRESET#
4.000MHZ
MA506
XTAL
EXTAL
XFC
XTAL
EXTAL
XFC
TRST
TCK/DSCK
PROCESSOR
TIMEBASE
SCH B SH.10


MPC855T-66MHz
PROCESSOR CONTROL
MEMORY CONTROL SIGNALS
WE0/BS_B0/IORD
WE1/BS_B1/IOWR
WE2/BS_B2/PCOE
WE3/BS_B3/PCWE
WE0#/BSB0#
WE1#/BSB1#
WE2#/BSB2#
WE3#/BSB3#
33 OHM,EXB-8V
GPL_A0/GPL_B0/CS0
GPL_A1/GPL_B1/CS1
GPL_A2/GPL_B2/CS2
GPL_A3/GPL_B3/CS3
GPL_A0#
GPL_A1#
GPL_A2#
GPL_A3#
PROCESSOR ADDRESS BUS
ADDR[31-0]
A0
ADDR31
ADDR3
A31
ADDR0
CS2
CS2#
CLKOUT
CLOCKOUT
OP3/MODCK2/DSDO
OP2/MODCK1/STS
MODCK2
MODCK1

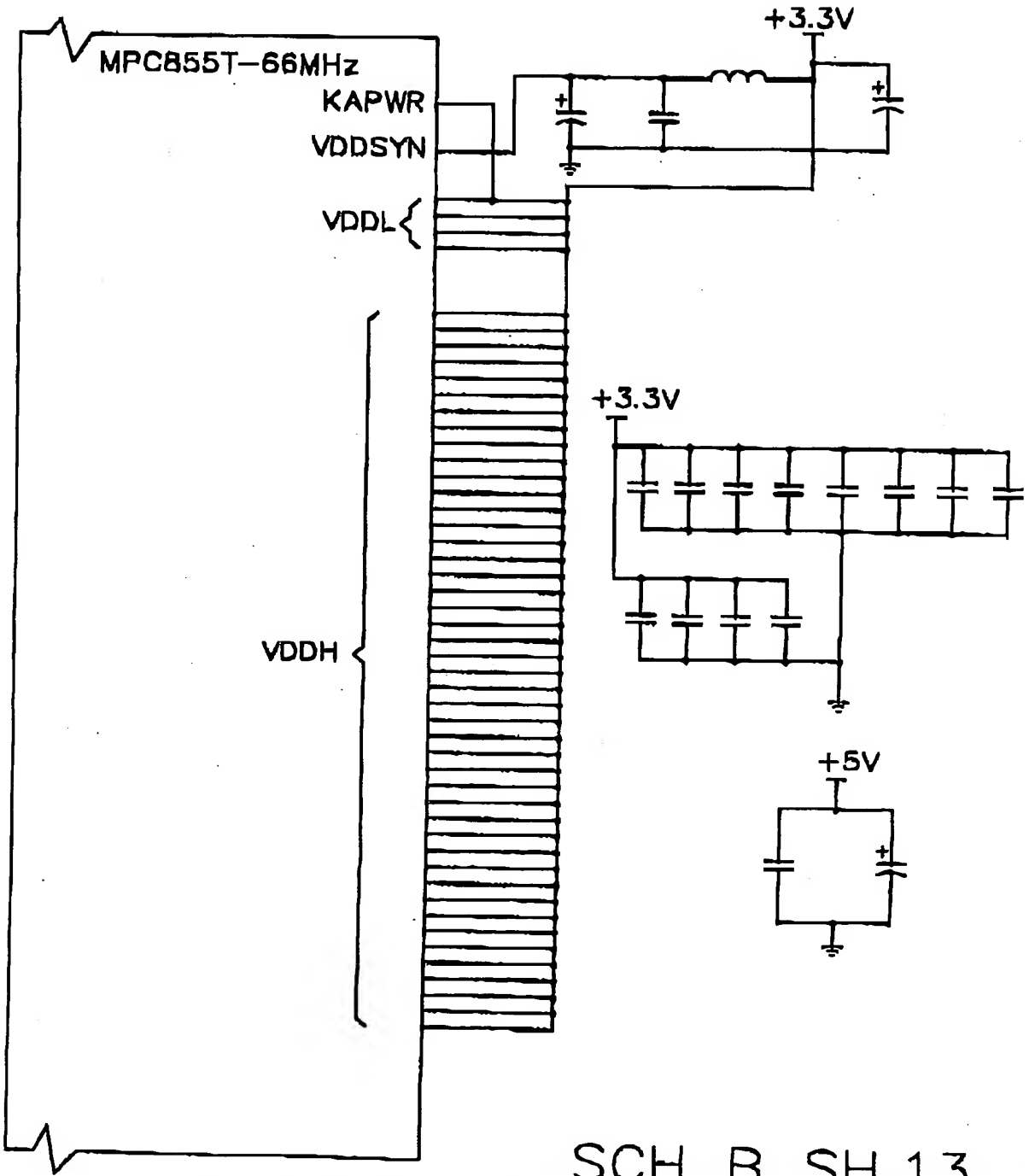
SCH B SH.11

FIG. 16S



CONTROLLER PROCESSOR GROUNDS

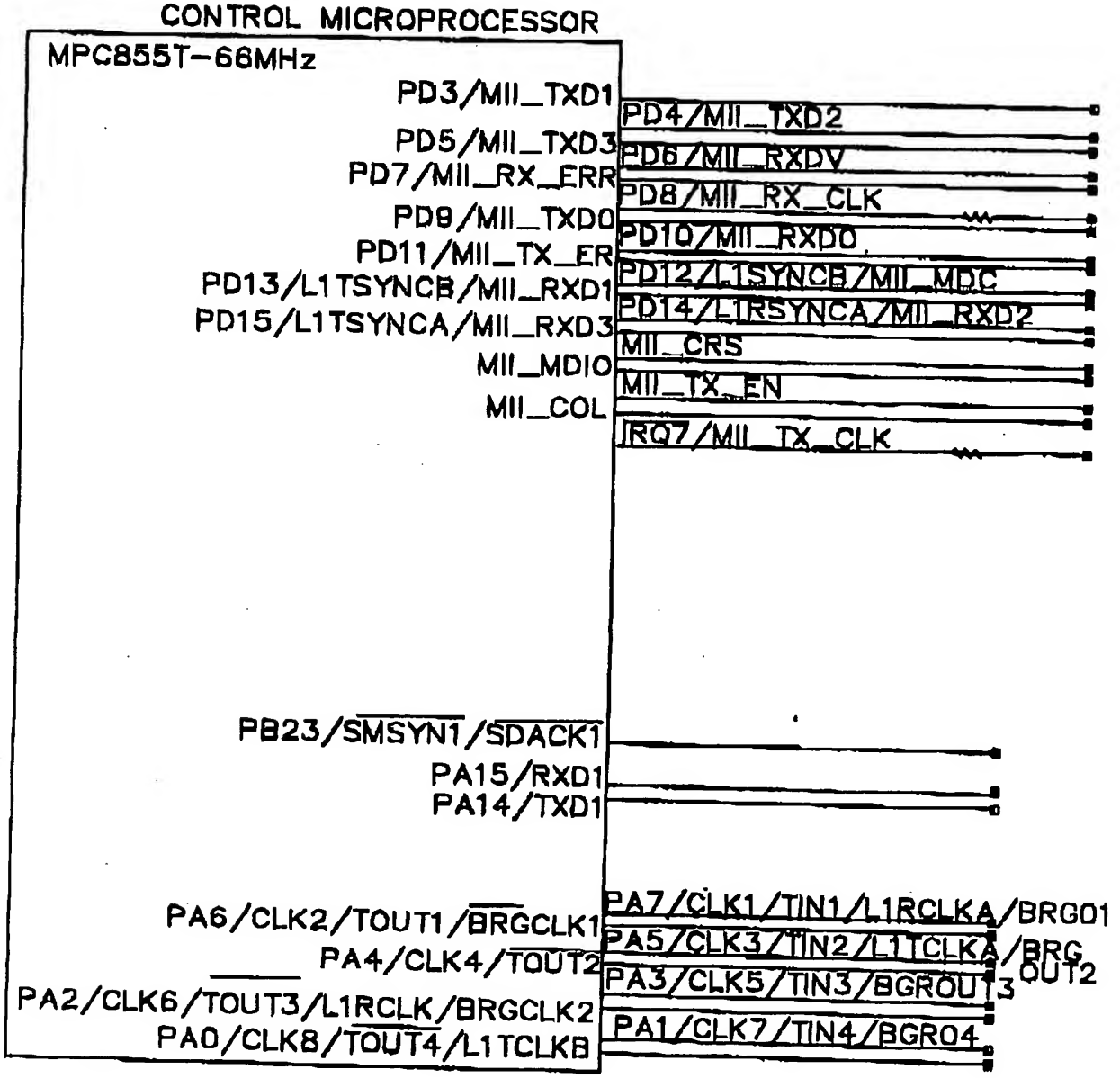
Fig 16.1



SCH B SH.13

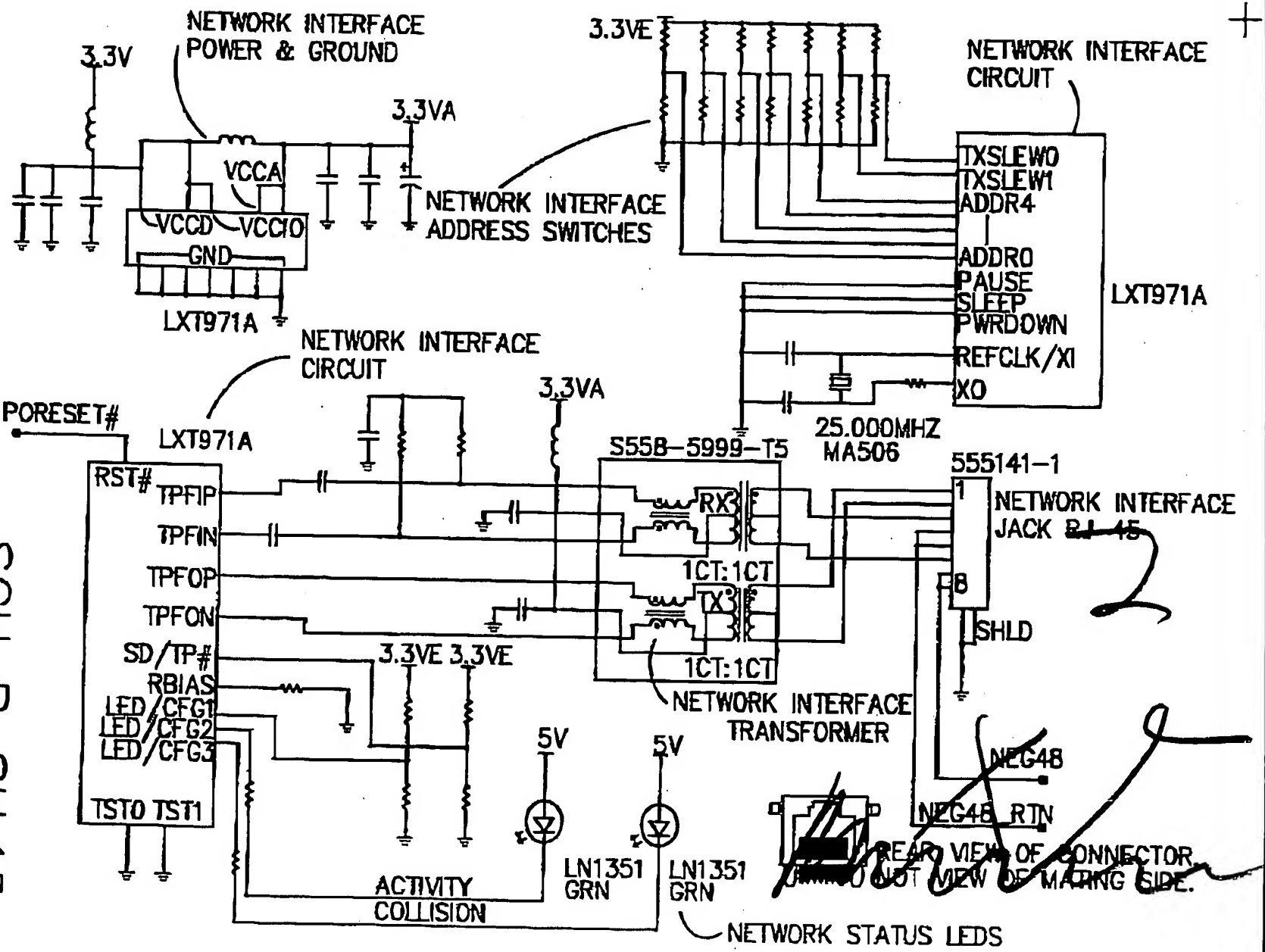
POWER CIRCUITS

CONTROL OF POWER


CONTROL MICROPROCESSOR
MPC855T-66MHz
PD3/MII_TXD1
PD4/MII_TXD2
PD5/MII_TXD3
PD6/MII_RXDV
PD7/MII_RX_ERR
PD8/MII_RX_CLK
PD9/MII_TXD0
PD10/MII_RXD0
PD11/MII_TX_ER
PD12/L1TSYNCB/MII_MDC
PD13/L1TSYNCB/MII_RXD1
PD14/L1RSYNCA/MII_RXD2
PD15/L1TSYNCA/MII_RXD3
MII_CRS
MII_MDIO
MII_TX_EN
MII_COL
IRQ7/MII_TX_CLK
PB23/SMSYN1/SDACK1
PA15/RXD1
PA14/TXD1
PA7/CLK1/TIN1/L1RCLKA/BRG01
PA6/CLK2/TOUT1/BRGCLK1
PA5/CLK3/TIN2/L1TCLKA/BRG
PA4/CLK4/TOUT2
OUT2
PA3/CLK5/TIN3/BGROUT3
PA2/CLK6/TOUT3/L1RCLK/BRGCLK2
PA1/CLK7/TIN4/BGR04
PA0/CLK8/TOUT4/L1TCLKB

SCH B SH.14

Fig 16V



SCH B SH.15

CONTROLLER LAN INTERFACE

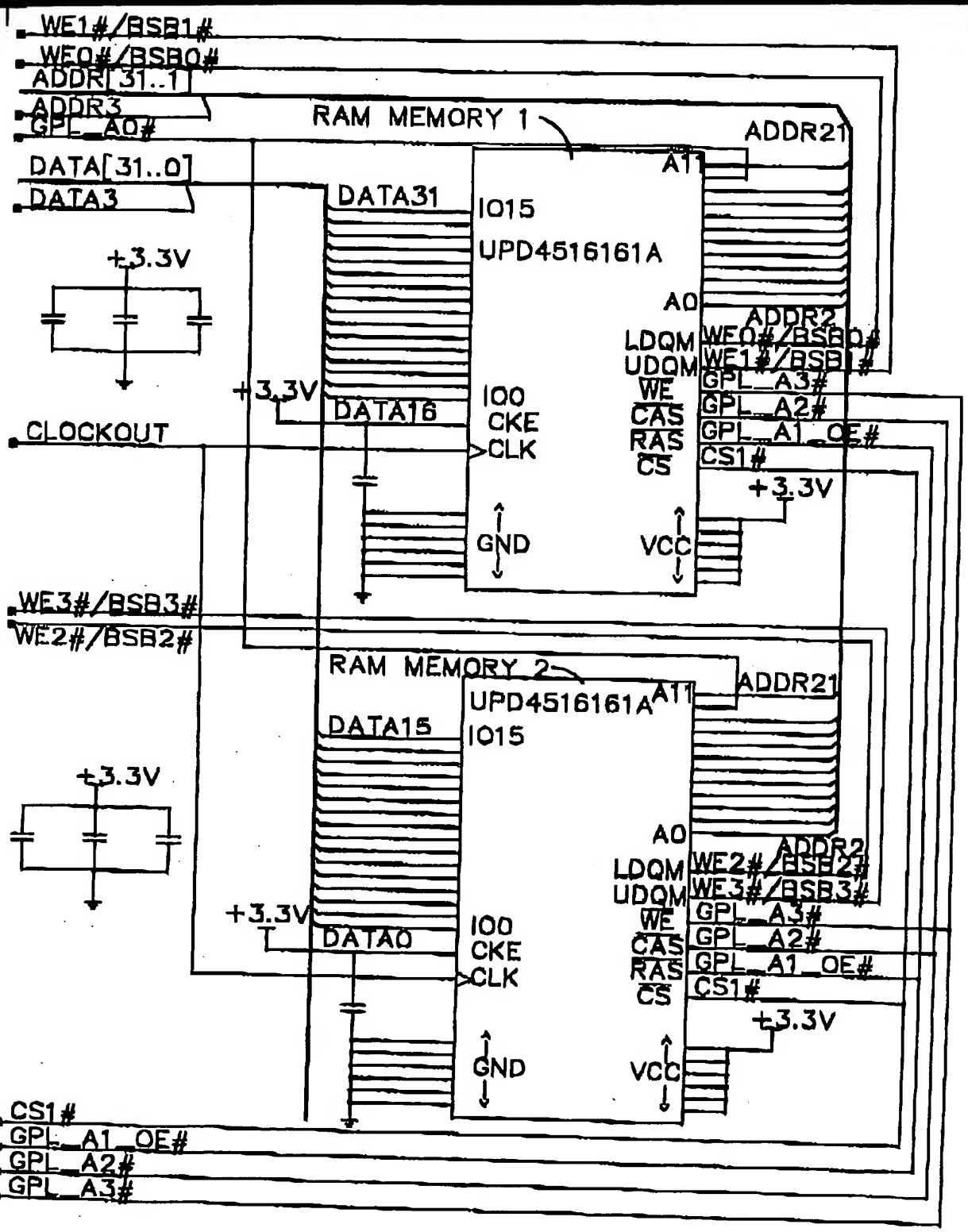
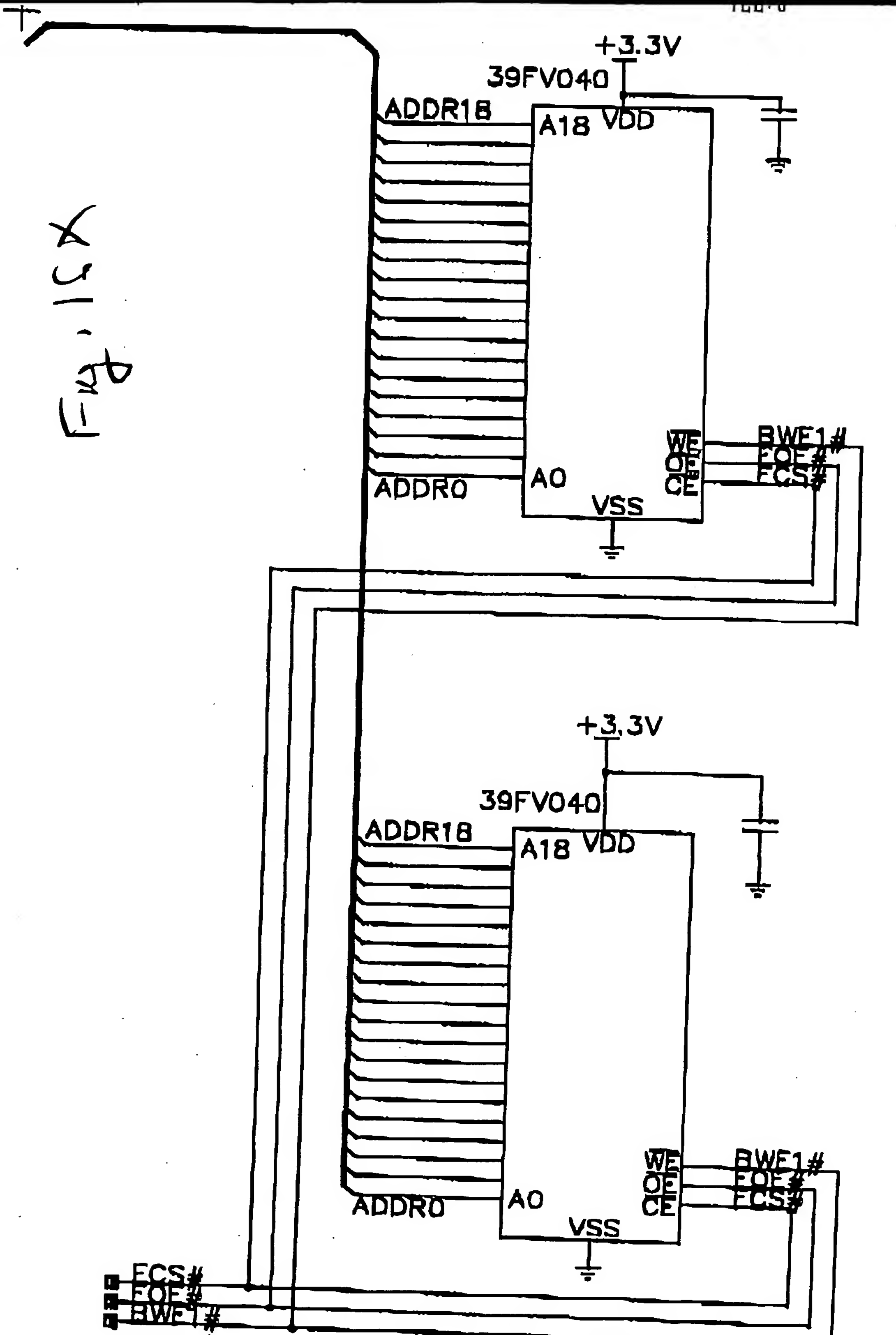


Fig. 16.3

COMMUNICATION PROCESSOR RAM

SCH B SH.16

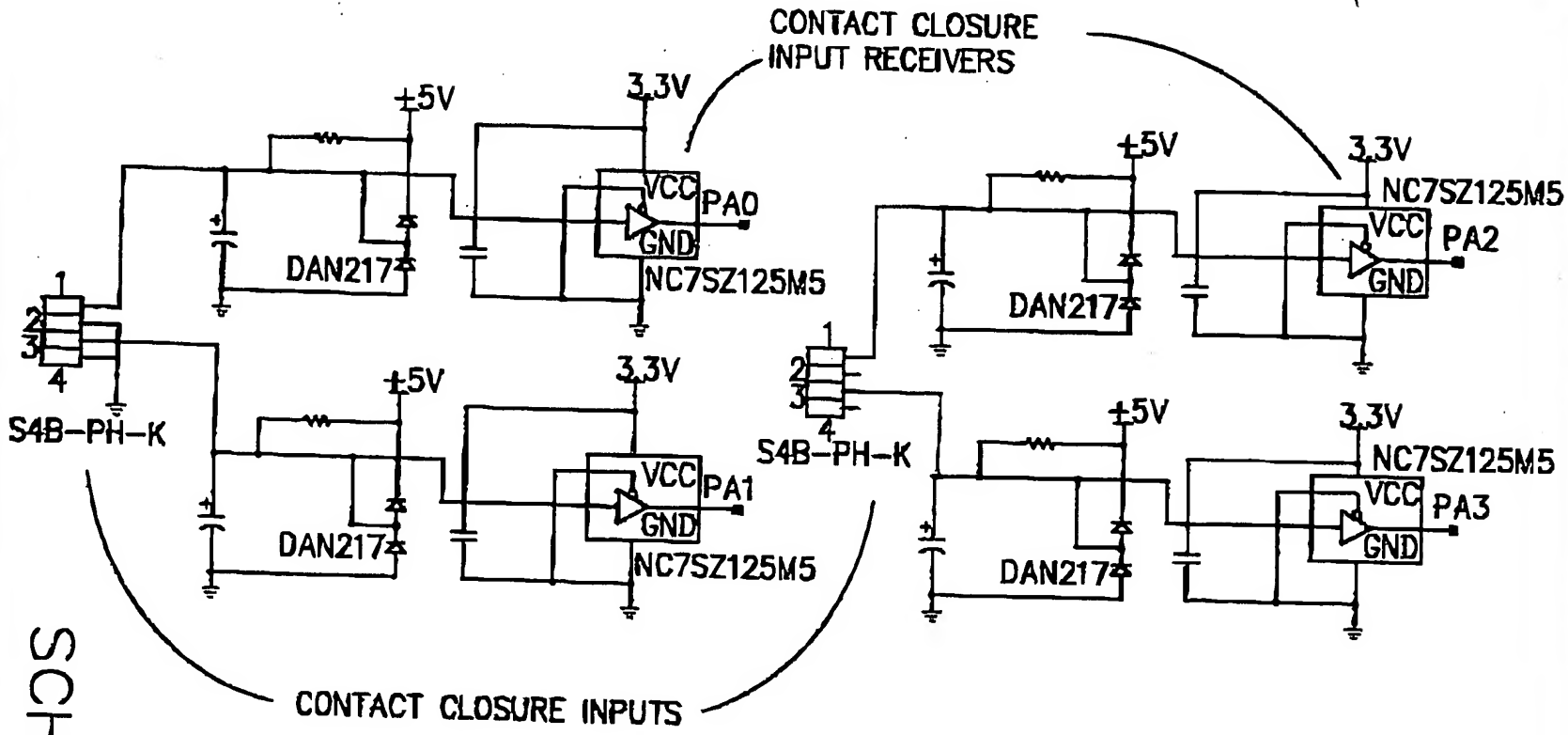
Fig. 15X



CONTROLLER PROCESSOR NON-VOLATILE MEMORY

SCH B SH.17

Fig. 16Y

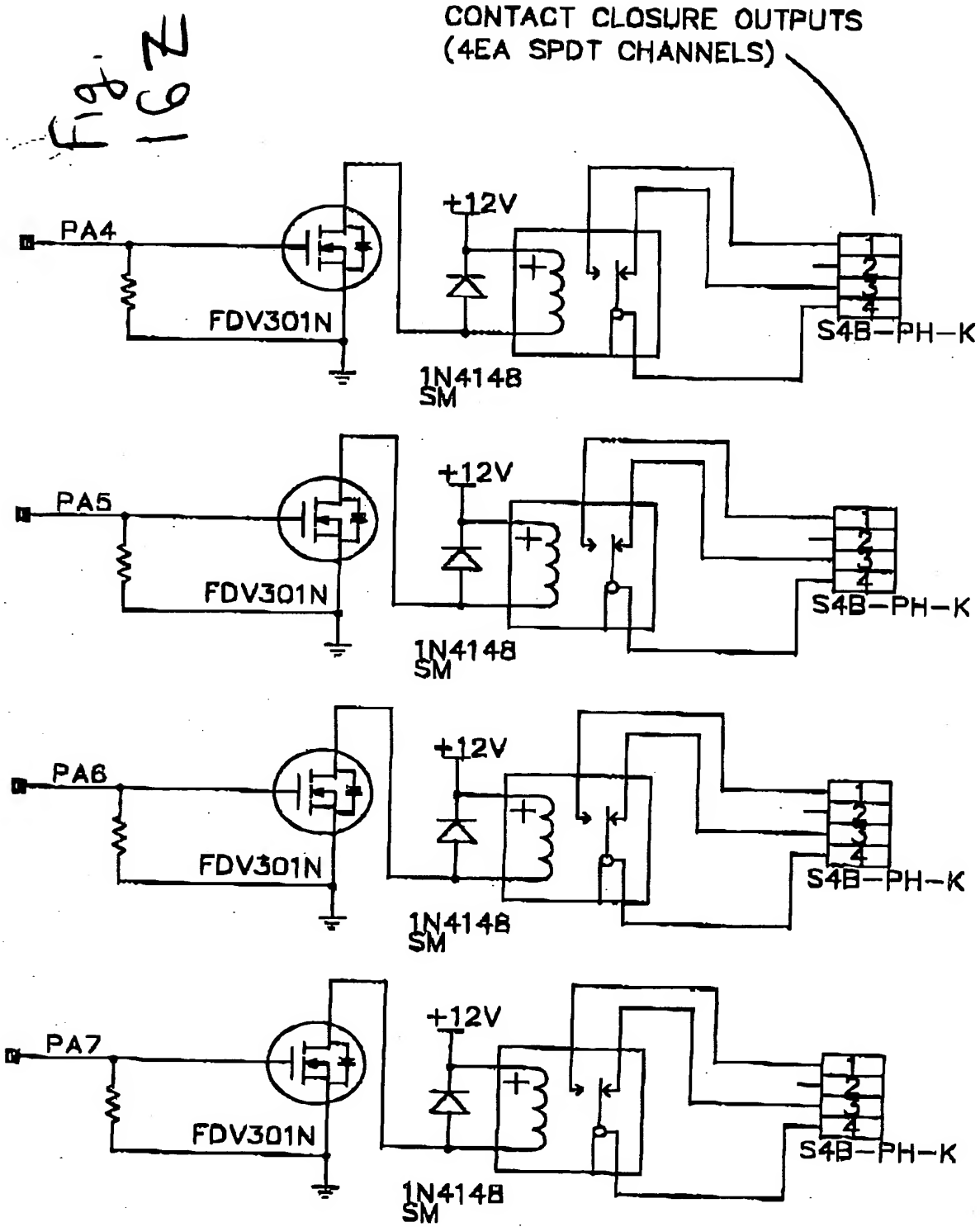


SCH 8 SH 8.00

DETECTION

CONTROLLER - EVENT INTERFACES

Fig 16

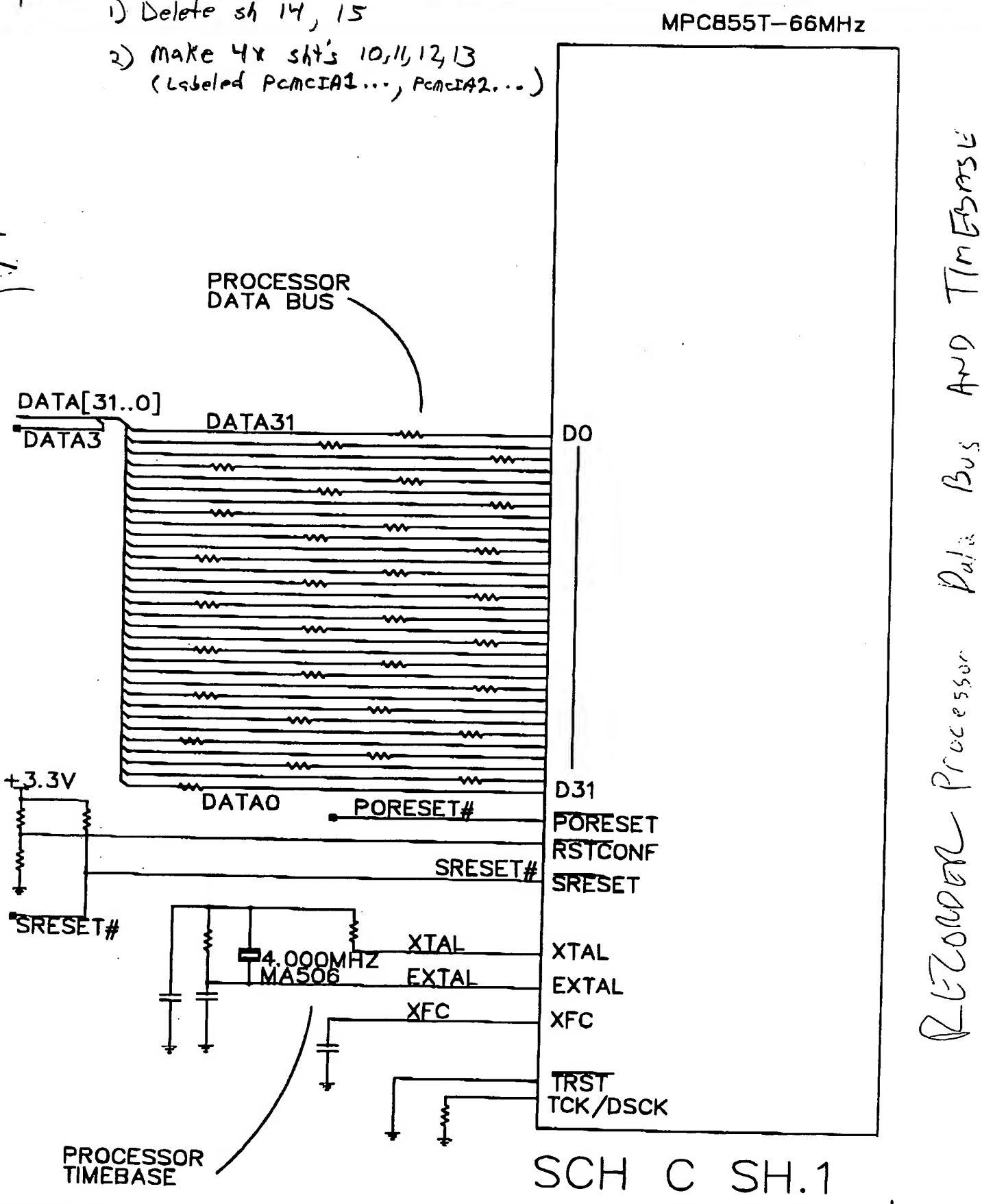


SCH B SH.9

CONTROLLER - OUTPUT INTERFACES

1) Delete sh 14, 15

2) make 4x sht's 10,11,12,13
(Labeled PcmcIA1..., PcmcIA2...)

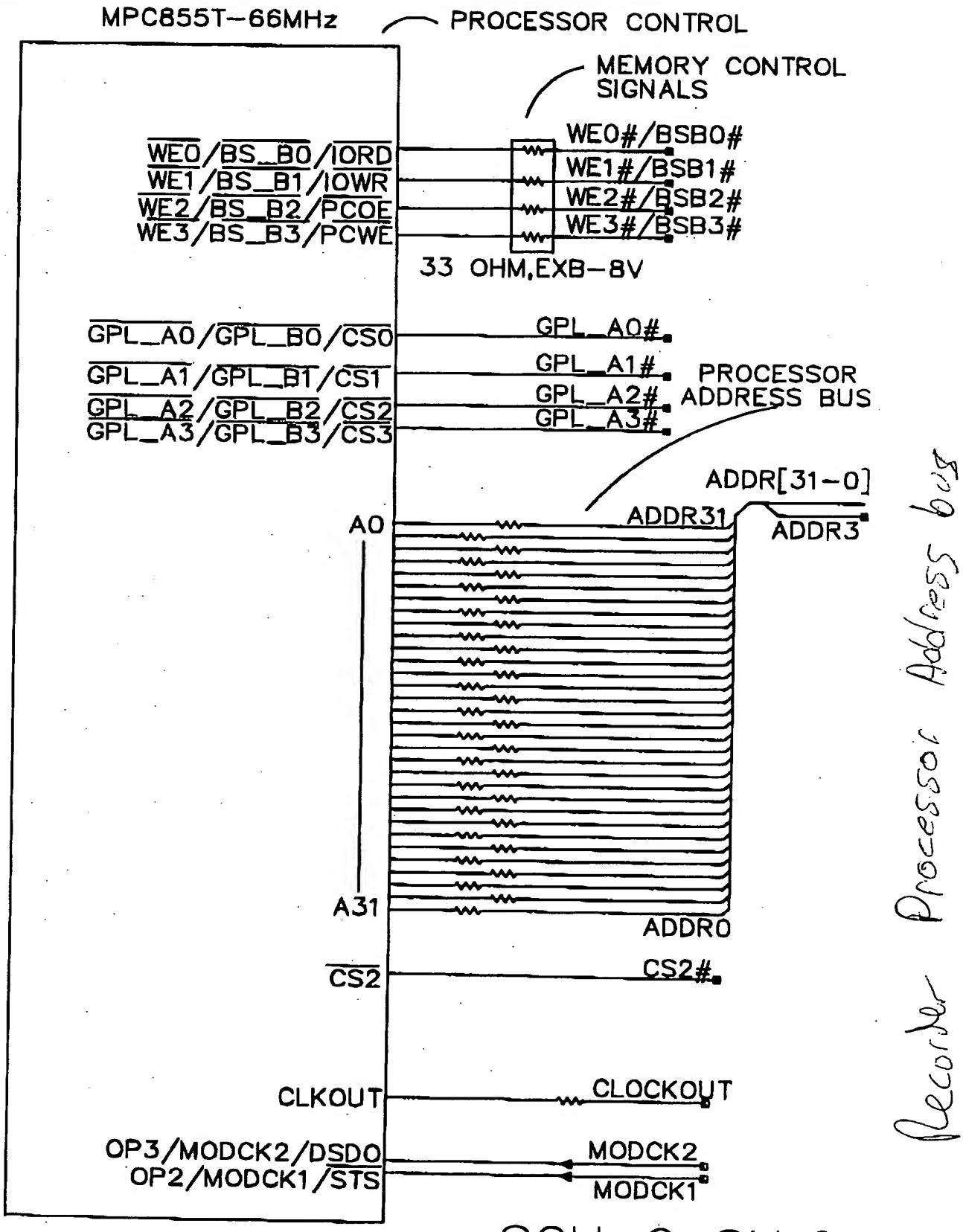


SCH C SH.1

Fig. 17A

Address Bus And Timebase Processor

Fig. 17B



Recorder Processor Address bus

SCH C SH.2

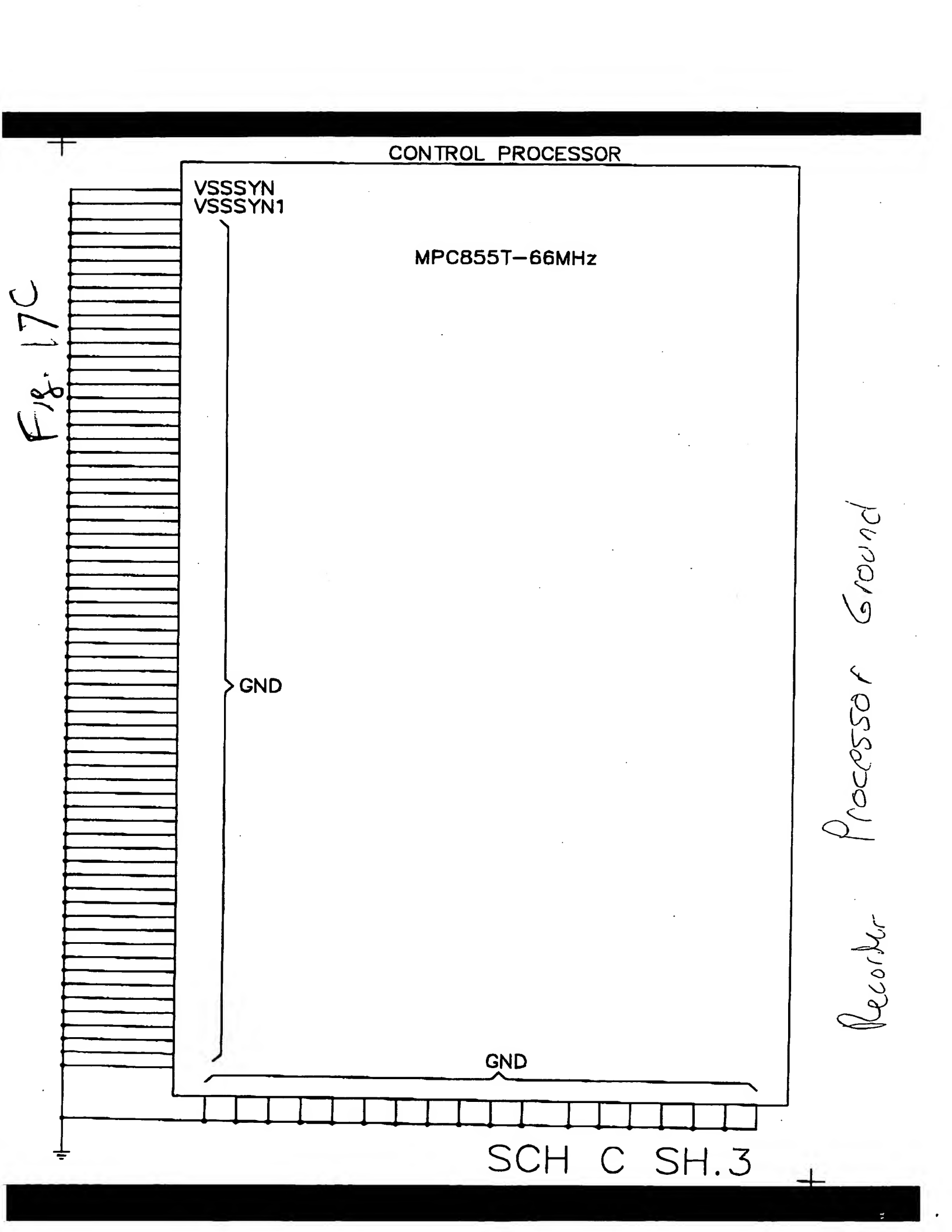
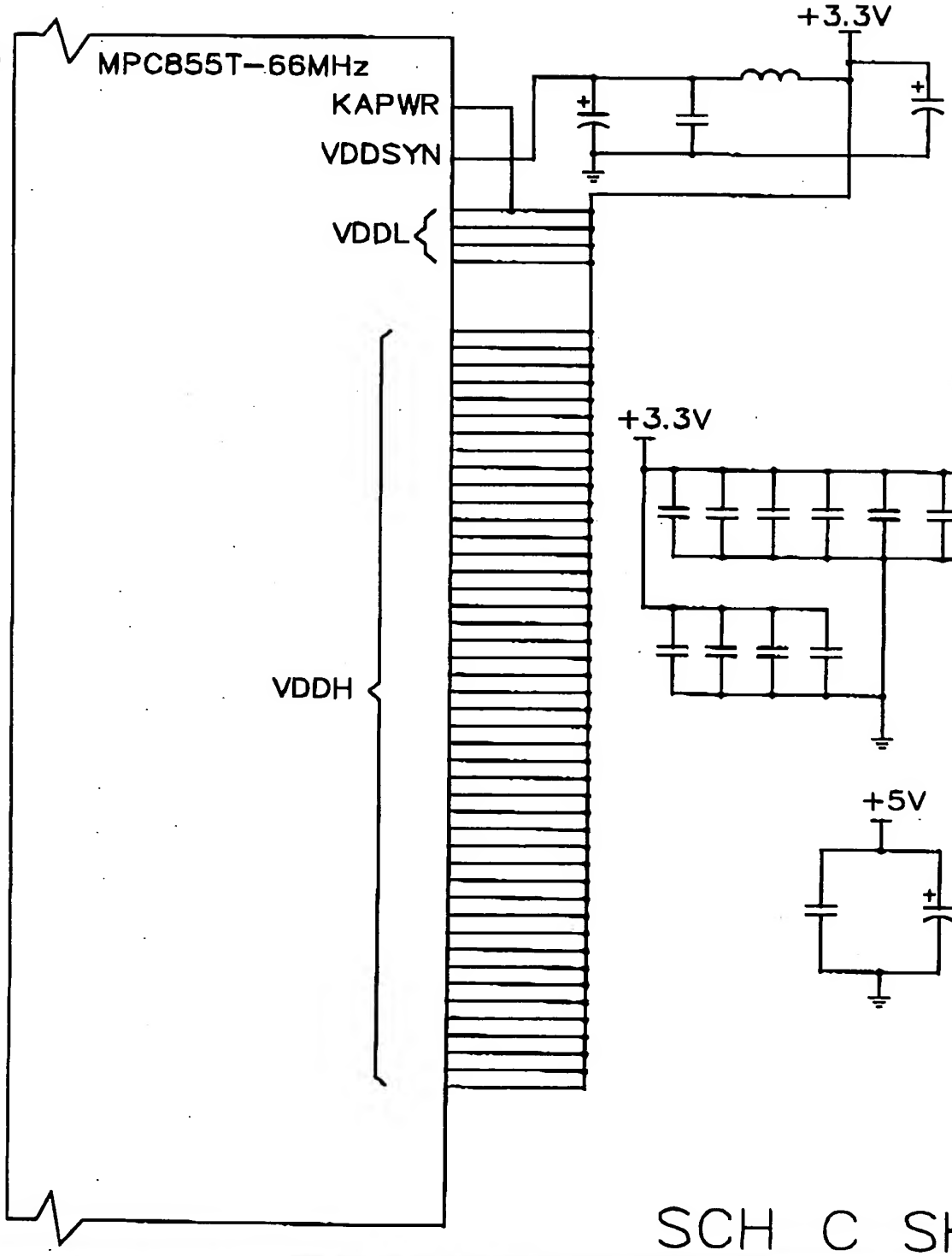

CONTROL PROCESSOR
VSSSYN
VSSSYN1
MPC855T–66MHz
GND
GND
SCH C SH.3
Fig. 17C
Processor Ground
Recorder

Fig. 17C

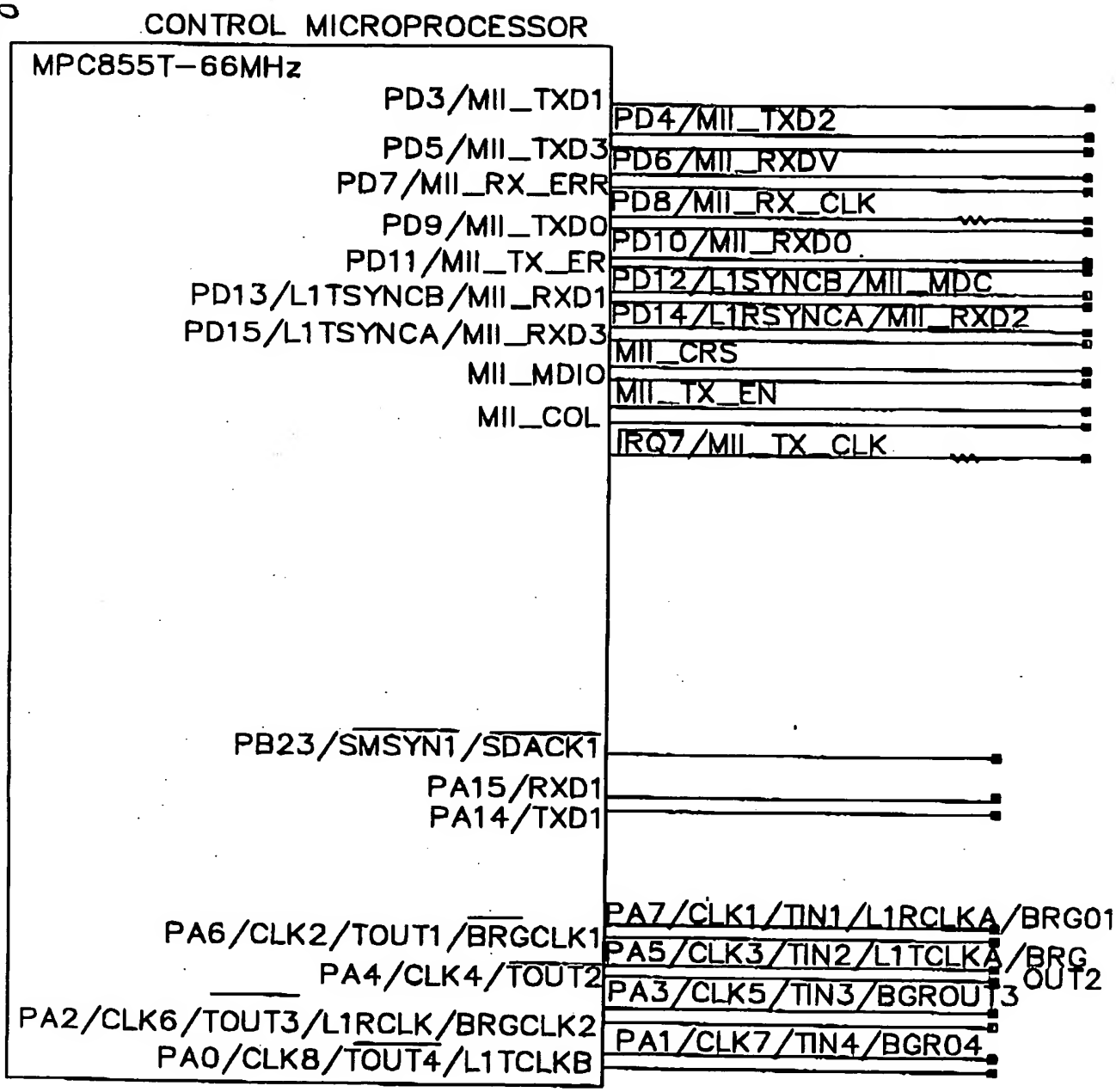


Processor V_{DD}

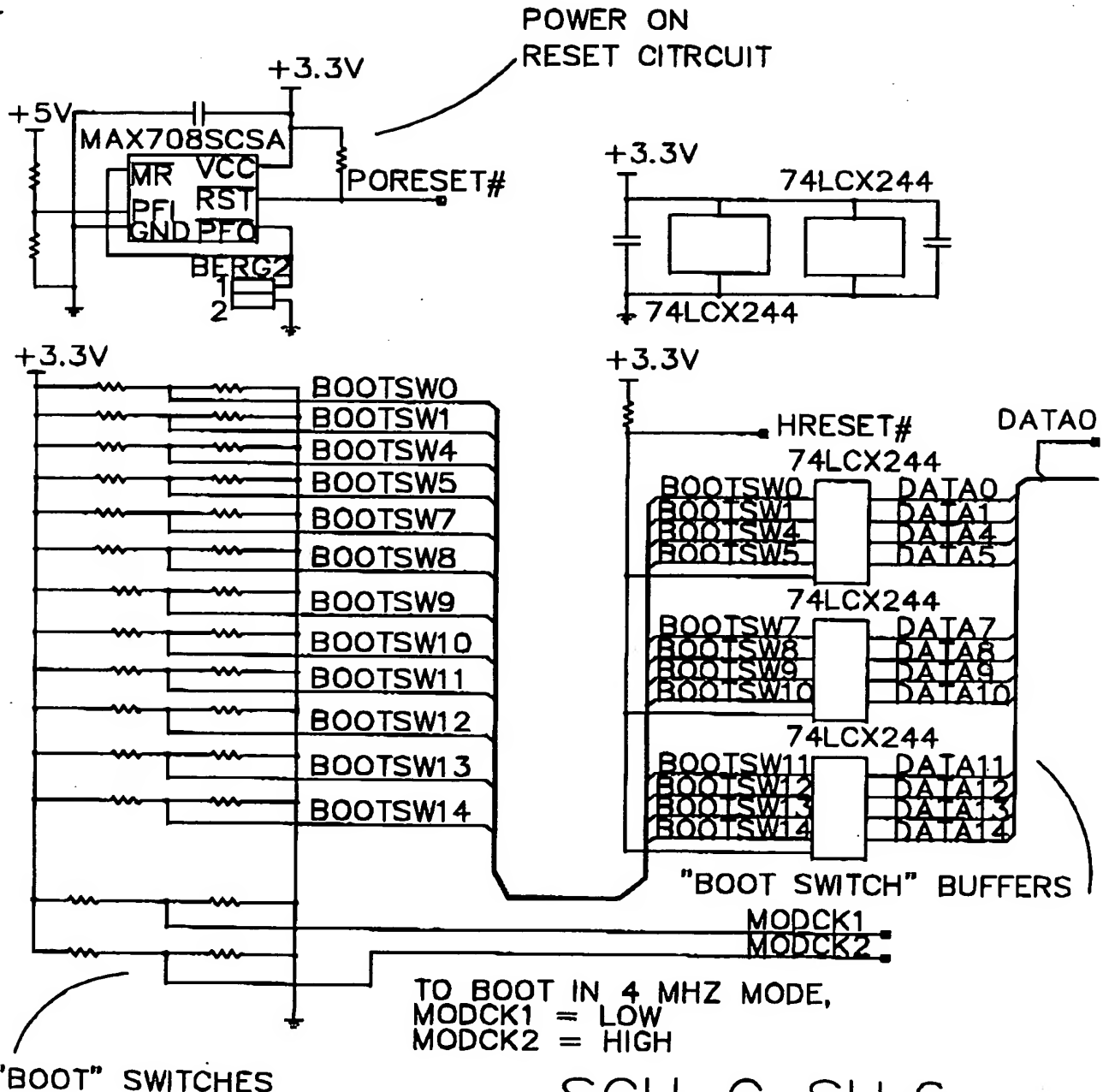
Recorder

SCH C SH.4

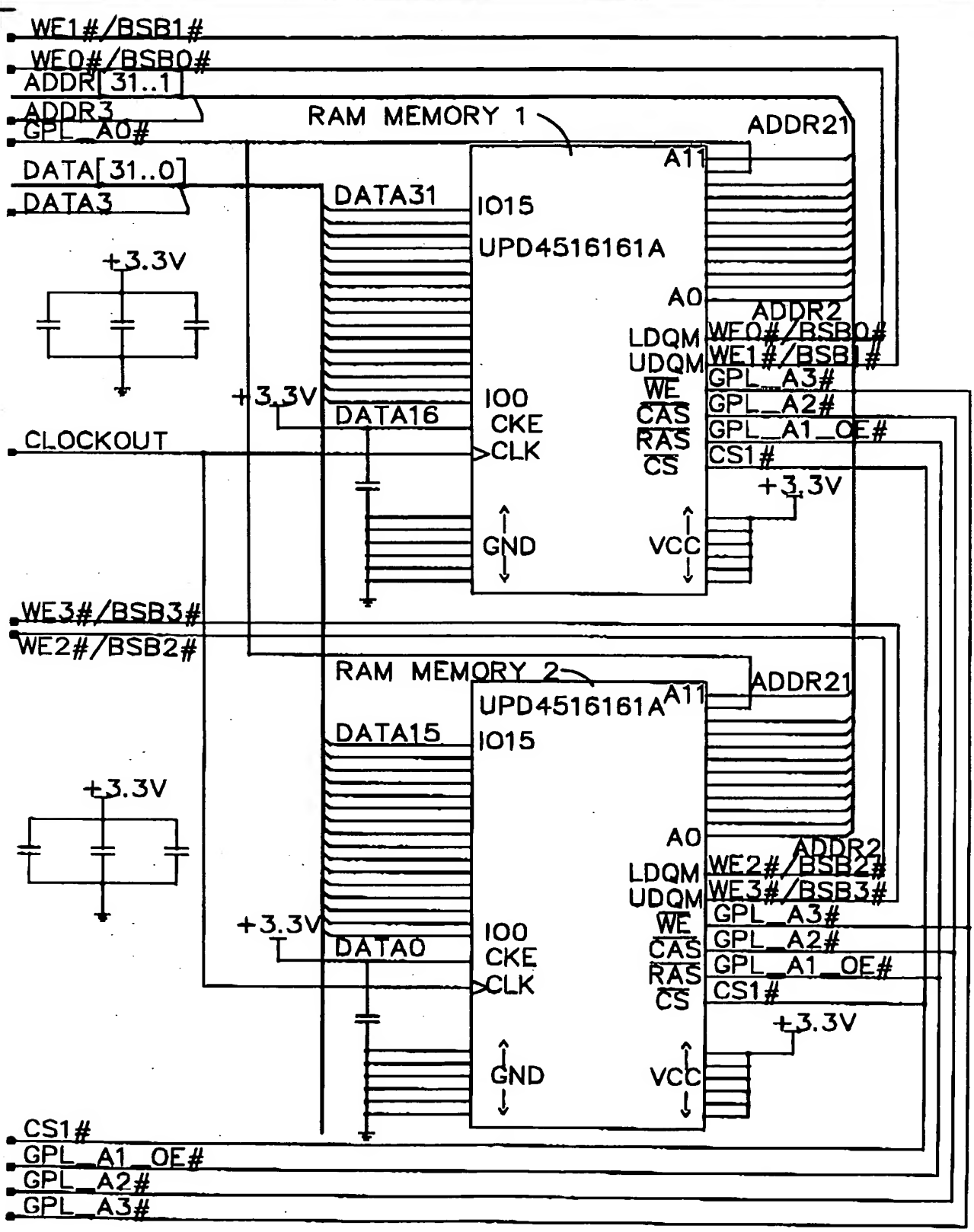
Fig. 17D



SCH C SH.5


POWER ON
RESET CITRCUIT
+3.3V
+5V
MAX708SCSA
MR VCC
PFI RST
GND PFO
PORESET#
BERG2
1
2
+3.3V
74LCX244
74LCX244
+3.3V
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
+3.3V
HRESET#
DATA0
74LCX244
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
DATA0
DATA1
DATA4
DATA5
74LCX244
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
DATA7
DATA8
DATA9
DATA10
74LCX244
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
DATA11
DATA12
DATA13
DATA14
"BOOT SWITCH" BUFFERS
MODCK1
MODCK2
TO BOOT IN 4 MHZ MODE,
MODCK1 = LOW
MODCK2 = HIGH
"BOOT" SWITCHES

SCH C SH.6


WE1#/BSB1#
WE0#/BSB0#
ADDR[31..1]
ADDR3
GPL_A0#
DATA[31..0]
DATA3
RAM MEMORY 1
ADDR21
A11
DATA31
IO15
UPD4516161A
A0
ADDR2
LDQM
WE0#/BSB0#
UDQM
WE1#/BSB1#
WE
GPL_A3#
CAS
GPL_A2#
RAS
GPL_A1_OE#
CS
CS1#
+3.3V
IO0
DATA16
CKE
CLK
CLOCKOUT
GND
VCC
WE3#/BSB3#
WE2#/BSB2#
RAM MEMORY 2
ADDR21
UPD4516161A
A11
DATA15
IO15
A0
ADDR2
WE2#/BSB2#
WE3#/BSB3#
GPL_A3#
GPL_A2#
GPL_A1_OE#
CS1#
+3.3V
IO0
DATA0
CKE
CLK
GND
VCC
CS1#
GPL_A1_OE#
GPL_A2#
GPL_A3#

SCH C SH.7

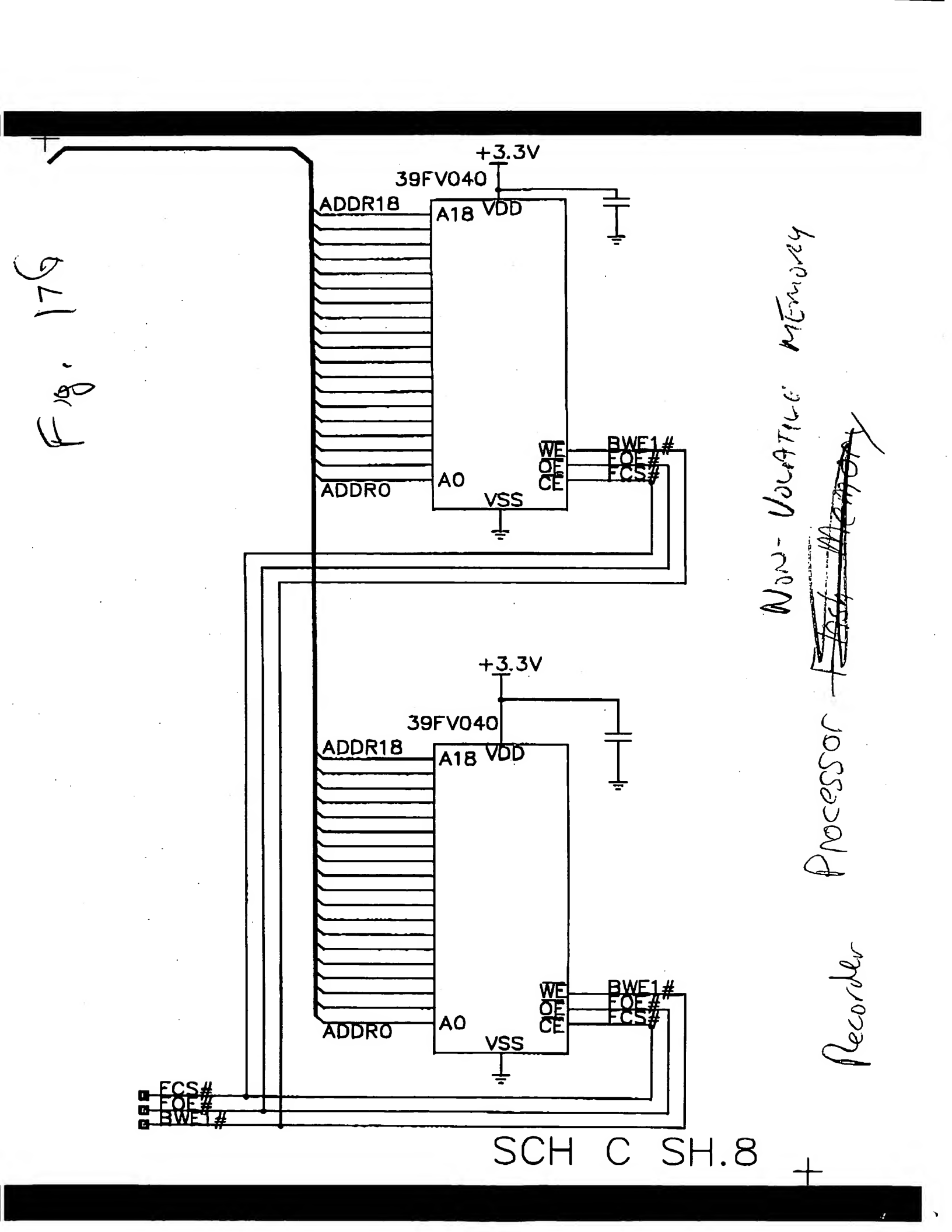


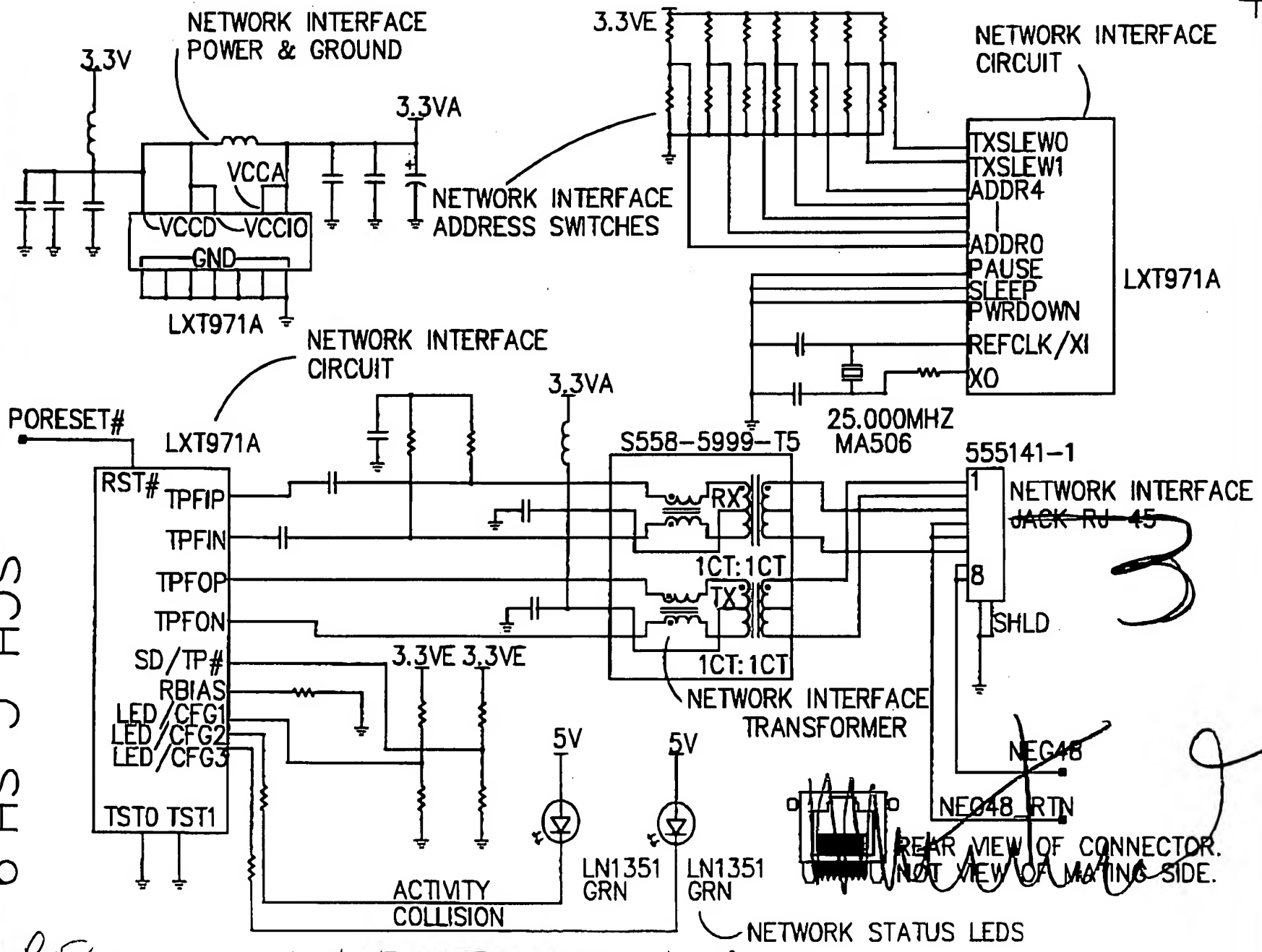
Fig. 17

Non-Volatile Memory

Processor

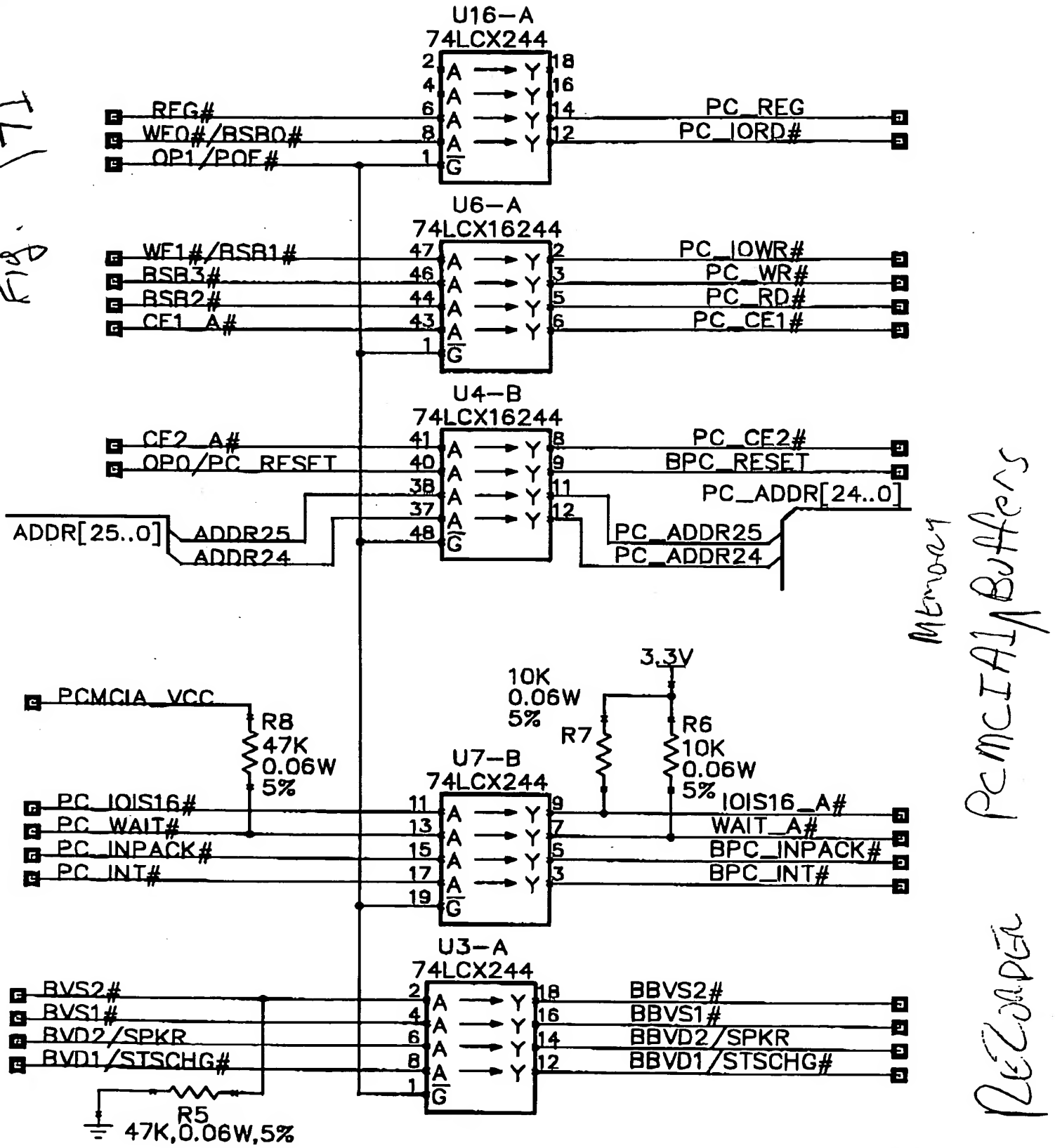
Recorder

Fig. 17A

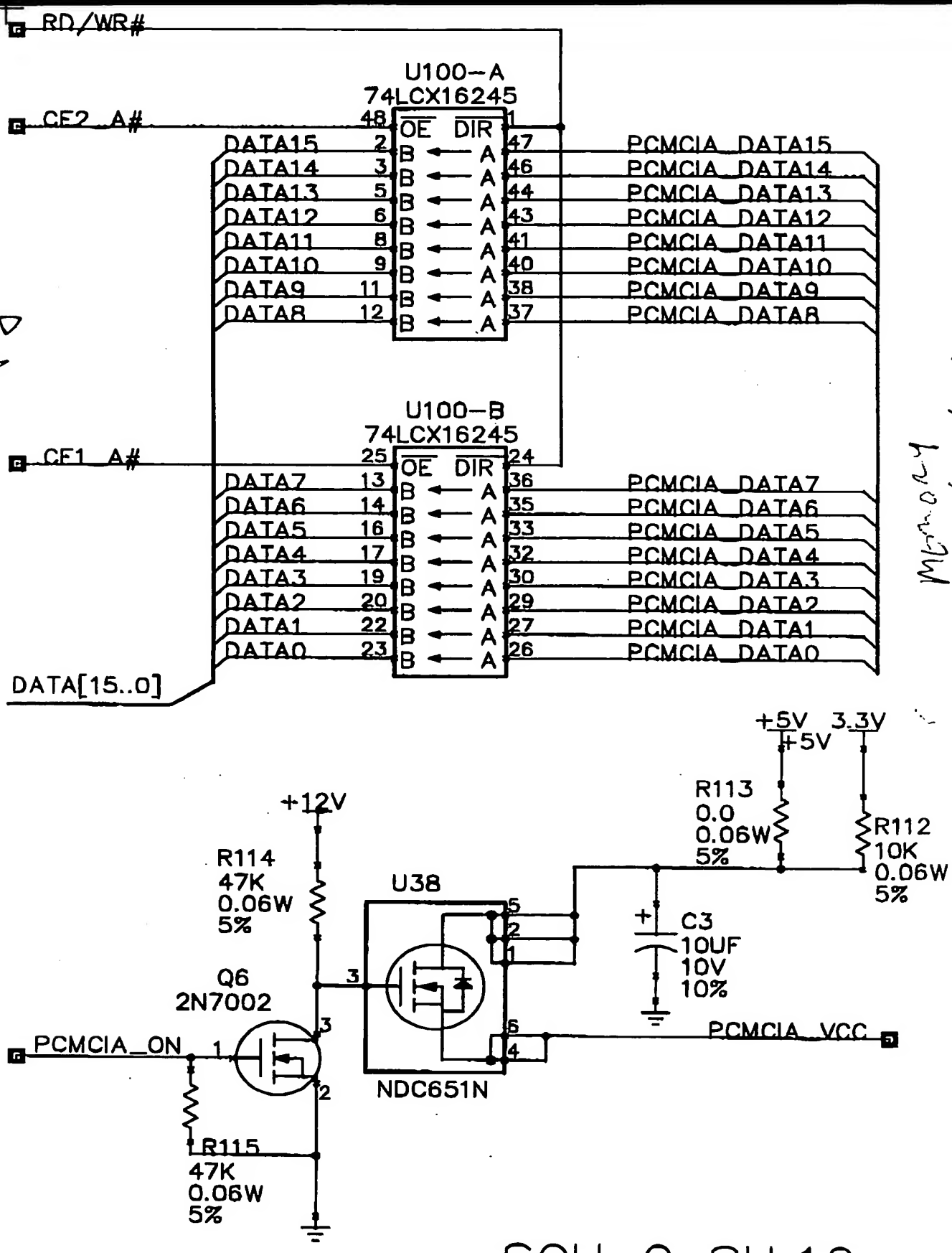


SCH C SH 9

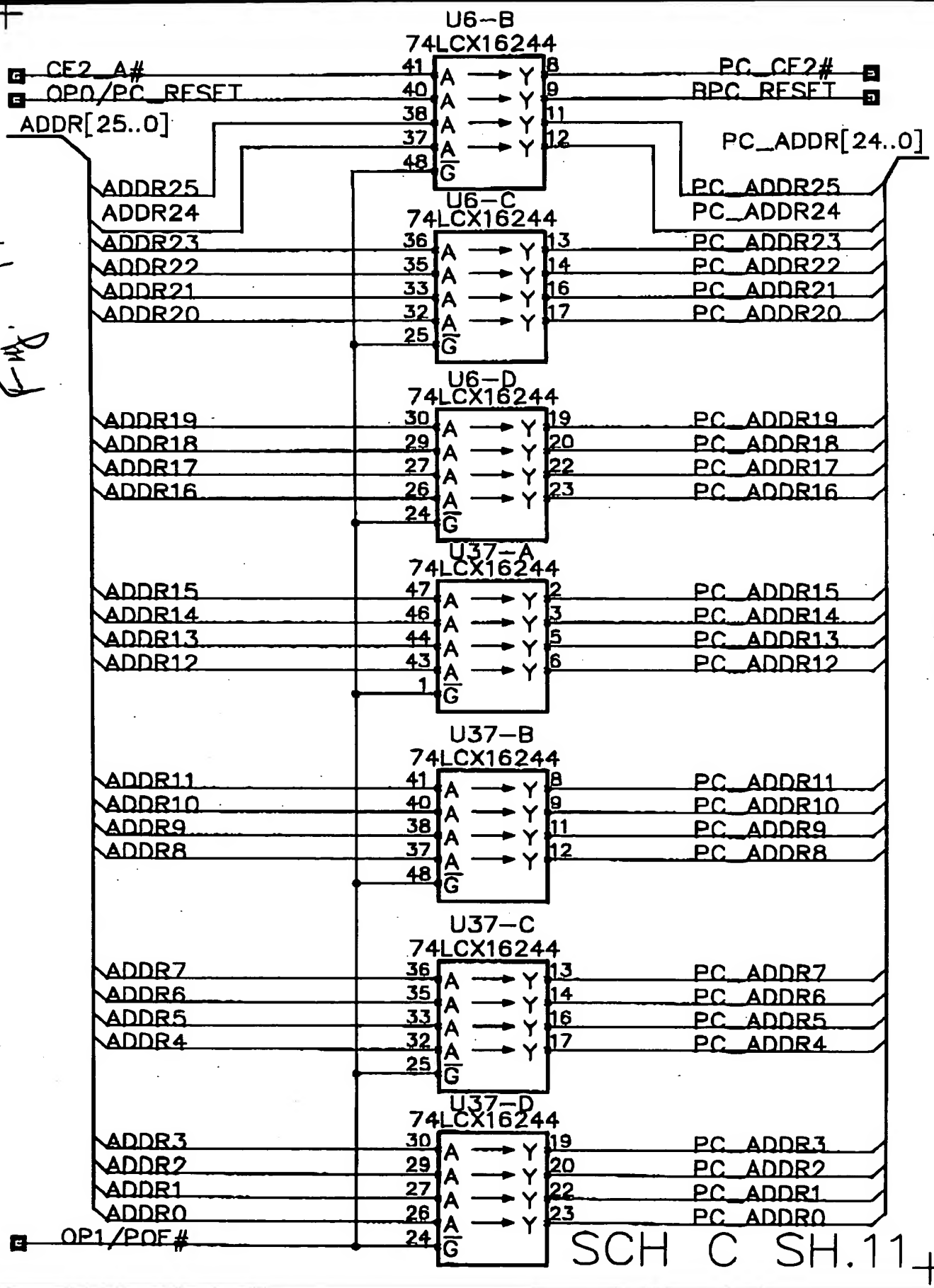
RECORDER LAN ~~Ethernet~~ Interface

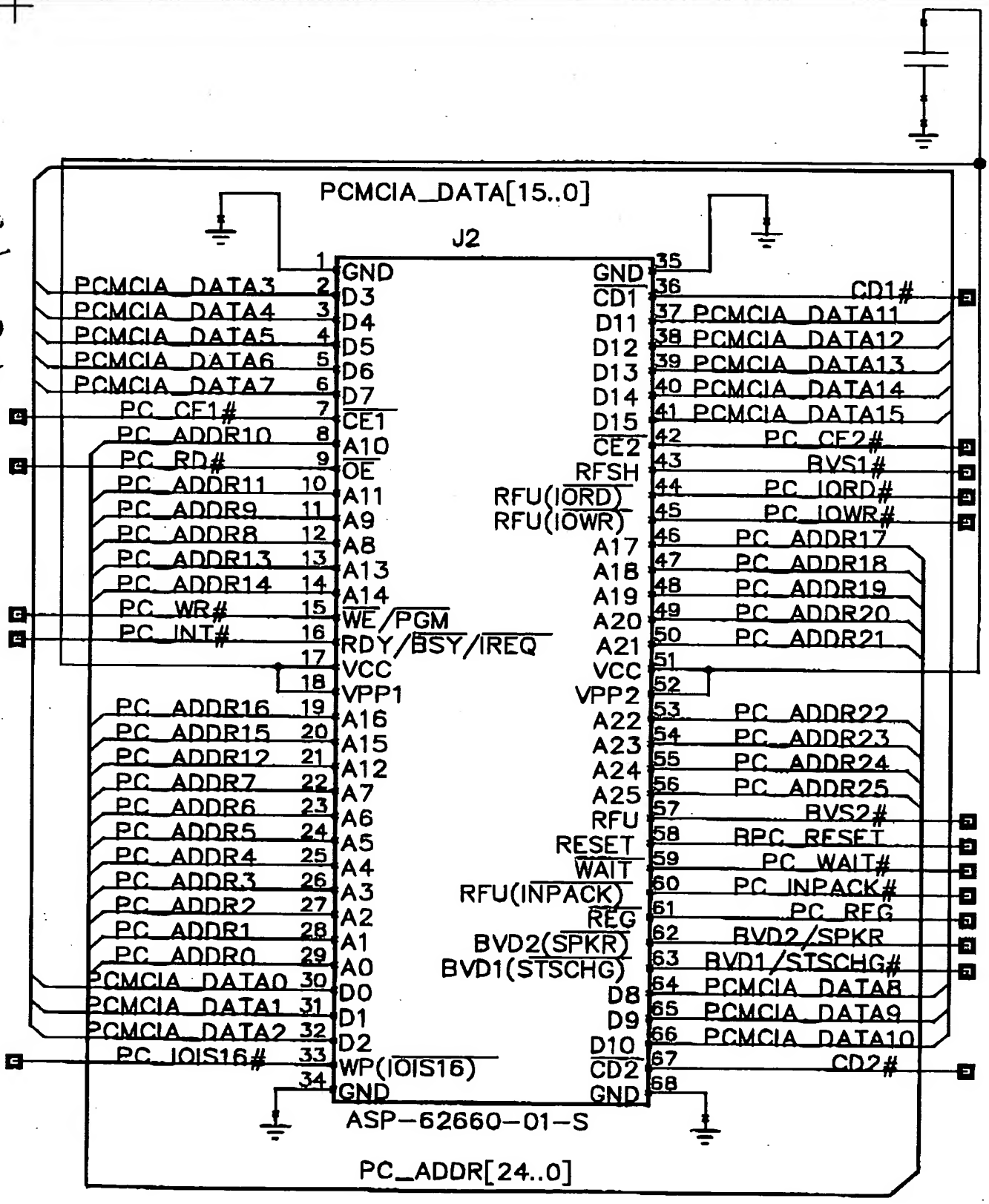

U16-A
74LCX244
REG#
WE0#/BSB0#
OP1/POE#
PC_REG
PC_IORD#
U6-A
74LCX16244
WE1#/BSB1#
BSB3#
BSB2#
CE1_A#
PC_IOWR#
PC_WR#
PC_RD#
PC_CE1#
U4-B
74LCX16244
CE2_A#
OP0/PC_RESET
ADDR[25..0]
ADDR25
ADDR24
PC_CE2#
BPC_RESET
PC_ADDR[24..0]
PC_ADDR25
PC_ADDR24
3.3V
10K
0.06W
5%
R7
R6
10K
0.06W
5%
PCMCIA_VCC
R8
47K
0.06W
5%
U7-B
74LCX244
PC_IOIS16#
PC_WAIT#
PC_INPACK#
PC_INT#
IOIS16_A#
WAIT_A#
BPC_INPACK#
BPC_INT#
U3-A
74LCX244
BVS2#
BVS1#
BVD2/SPKR
BVD1/STSCHG#
BBVS2#
BBVS1#
BBVD2/SPKR
BBVD1/STSCHG#
R5
47K,0.06W,5%

SCH C SH.10


RD/WR#
U100-A
74LCX16245
CE2_A#
OE DIR
DATA15 2 B A 47 PCMCIA_DATA15
DATA14 3 B A 46 PCMCIA_DATA14
DATA13 5 B A 44 PCMCIA_DATA13
DATA12 6 B A 43 PCMCIA_DATA12
DATA11 8 B A 41 PCMCIA_DATA11
DATA10 9 B A 40 PCMCIA_DATA10
DATA9 11 B A 38 PCMCIA_DATA9
DATA8 12 B A 37 PCMCIA_DATA8
U100-B
74LCX16245
CE1_A#
OE DIR
DATA7 13 B A 36 PCMCIA_DATA7
DATA6 14 B A 35 PCMCIA_DATA6
DATA5 16 B A 33 PCMCIA_DATA5
DATA4 17 B A 32 PCMCIA_DATA4
DATA3 19 B A 30 PCMCIA_DATA3
DATA2 20 B A 29 PCMCIA_DATA2
DATA1 22 B A 27 PCMCIA_DATA1
DATA0 23 B A 26 PCMCIA_DATA0
DATA[15..0]
+5V
3.3V
+5V
R113
0.0
0.06W
5%
R112
10K
0.06W
5%
+12V
R114
47K
0.06W
5%
U38
C3
10UF
10V
10%
Q6
2N7002
PCMCIA_ON
PCMCIA_VCC
R115
47K
0.06W
5%
NDC651N

SCH C SH.12


U6-B
74LCX16244
CE2_A#
OP0/PC_RESET
ADDR[25..0]
PC_CE2#
BPC_RESET
PC_ADDR[24..0]
ADDR25
ADDR24
U6-C
74LCX16244
ADDR23
ADDR22
ADDR21
ADDR20
PC_ADDR25
PC_ADDR24
PC_ADDR23
PC_ADDR22
PC_ADDR21
PC_ADDR20
U6-D
74LCX16244
ADDR19
ADDR18
ADDR17
ADDR16
PC_ADDR19
PC_ADDR18
PC_ADDR17
PC_ADDR16
U37-A
74LCX16244
ADDR15
ADDR14
ADDR13
ADDR12
PC_ADDR15
PC_ADDR14
PC_ADDR13
PC_ADDR12
U37-B
74LCX16244
ADDR11
ADDR10
ADDR9
ADDR8
PC_ADDR11
PC_ADDR10
PC_ADDR9
PC_ADDR8
U37-C
74LCX16244
ADDR7
ADDR6
ADDR5
ADDR4
PC_ADDR7
PC_ADDR6
PC_ADDR5
PC_ADDR4
U37-D
74LCX16244
ADDR3
ADDR2
ADDR1
ADDR0
OP1/PDF#
PC_ADDR3
PC_ADDR2
PC_ADDR1
PC_ADDR0
SCH C SH.11


PCMCIA_DATA[15..0]
J2
1 GND
PCMCIA_DATA3 2 D3
PCMCIA_DATA4 3 D4
PCMCIA_DATA5 4 D5
PCMCIA_DATA6 5 D6
PCMCIA_DATA7 6 D7
PC_CE1# 7 CE1
PC_ADDR10 8 A10
PC_RD# 9 OE
PC_ADDR11 10 A11
PC_ADDR9 11 A9
PC_ADDR8 12 A8
PC_ADDR13 13 A13
PC_ADDR14 14 A14
PC_WR# 15 WE/PGM
PC_INT# 16 RDY/BSY/IREQ
17 VCC
18 VPP1
PC_ADDR16 19 A16
PC_ADDR15 20 A15
PC_ADDR12 21 A12
PC_ADDR7 22 A7
PC_ADDR6 23 A6
PC_ADDR5 24 A5
PC_ADDR4 25 A4
PC_ADDR3 26 A3
PC_ADDR2 27 A2
PC_ADDR1 28 A1
PC_ADDR0 29 A0
PCMCIA_DATA0 30 D0
PCMCIA_DATA1 31 D1
PCMCIA_DATA2 32 D2
PC_IOIS16# 33 WP(IOIS16)
34 GND
35 GND
36 CD1 CD1#
37 D11 PCMCIA_DATA11
38 D12 PCMCIA_DATA12
39 D13 PCMCIA_DATA13
40 D14 PCMCIA_DATA14
41 D15 PCMCIA_DATA15
42 CE2 PC_CE2#
43 RFSH BVS1#
44 RFU(IORD) PC_IORD#
45 RFU(IOWR) PC_IOWR#
46 A17 PC_ADDR17
47 A18 PC_ADDR18
48 A19 PC_ADDR19
49 A20 PC_ADDR20
50 A21 PC_ADDR21
51 VCC
52 VPP2
53 A22 PC_ADDR22
54 A23 PC_ADDR23
55 A24 PC_ADDR24
56 A25 PC_ADDR25
57 RFU BVS2#
58 RESET RPC_RESET
59 WAIT PC_WAIT#
60 RFU(INPACK) PC_INPACK#
61 REG PC_REG
62 BVD2(SPKR) BVD2/SPKR
63 BVD1(STSCHG) BVD1/STSCHG#
64 D8 PCMCIA_DATA8
65 D9 PCMCIA_DATA9
66 D10 PCMCIA_DATA10
67 CD2 CD2#
68 GND
ASP-62660-01-S
PC_ADDR[24..0]

SCH C SH.13